

# MAS6181

This is preliminary information on a new product under development. Micro Analog Systems Oy reserves the right to make any changes without notice.

## AM Receiver IC

*Preliminary*

- Dual Band Receiver IC
- High Sensitivity
- Very Low Power Consumption
- Wide Supply Voltage Range
- Power Down Control
- Control for AGC On
- High Selectivity by Crystal Filter
- Fast Startup Feature

### DESCRIPTION

The MAS6181 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiving. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain

control) can be used to switch AGC on or off if necessary. MAS6181 supports up to two frequency band operation by switching between two crystal filters and an additional antenna tuning capacitor.

MAS6181 has differential input and two internal compensation capacitor options for compensating shunt capacitances of different crystals (See ordering information on page 13).

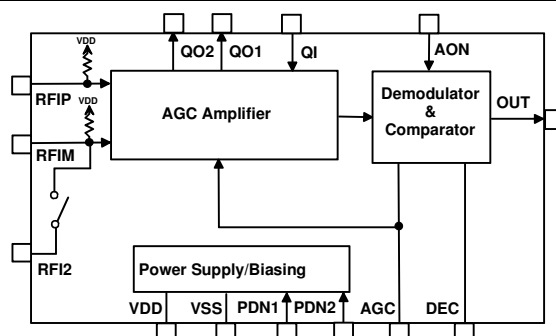
### FEATURES

- Dual Band Receiver IC
- Highly Sensitive AM Receiver, 0.4  $\mu\text{V}_{\text{RMS}}$  typ.
- Wide Supply Voltage Range from 1.1 V to 3.6 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter
- Differential Input

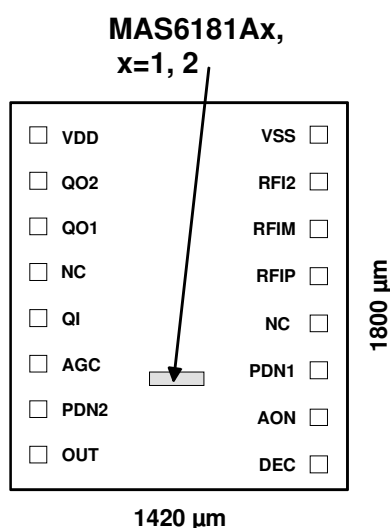
### APPLICATIONS

- Multi Band Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany), MSF (UK), HBG (Switzerland) and BPC (China)

### BLOCK DIAGRAM



## PAD LAYOUT



DIE size = 1.42 x 1.80 mm; rectangular PAD 80 μm x 80 μm

**Note:** Because the substrate of the die is internally connected to VSS, the die has to be connected to VSS or left floating. Please make sure that VSS is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

**Note:** Coordinates are pad center points where origin has been located in bottom-left corner of the silicon die.

Pad Identification	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	154 μm	1580 μm	
Quartz Filter Output for Crystal 2	QO2	154 μm	1393 μm	
Quartz Filter Output for Crystal 1	QO1	154 μm	1207 μm	
Not Connected	NC	154 μm	1021 μm	1
Quartz Filter Input for Crystals	QI	154 μm	835 μm	
AGC Capacitor	AGC	154 μm	648 μm	
Power Down/Frequency Selection Input 2	PDN2	154 μm	462 μm	2
Receiver Output	OUT	154 μm	276 μm	3
Demodulator Capacitor	DEC	1266 μm	276 μm	
AGC On Control	AON	1266 μm	462 μm	4
Power Down/Frequency Selection Input 1	PDN1	1266 μm	648 μm	2
Not Connected	NC	1266 μm	835 μm	1
Positive Receiver Input	RFIP	1266 μm	1021 μm	5
Negative Receiver Input	RFIM	1266 μm	1207 μm	5
Receiver Input 2 (for Antenna Capacitor 2)	RFI2	1266 μm	1393 μm	
Power Supply Ground	VSS	1266 μm	1580 μm	

### Notes:

- NC pads are not connected and they should be neglected.
- PDN1 = VDD and PDN2 = VDD means receiver off
  - Fast start-up is triggered when the receiver is after power down controlled to power up
- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
  - the output is a current source/sink with  $|I_{OUT}| > 5 \mu A$
  - at power down the output is pulled to VSS (pull down switch)
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
  - Internal pull-up with current  $< 1 \mu A$  which is switched off at power down
- Receiver inputs RFIP and RFIM have both 600 kΩ biasing resistors towards VDD

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	$V_{DD}-V_{SS}$		-0.3	5.5	V
Input Voltage	$V_{IN}$		$V_{SS}-0.3$	$V_{DD}+0.3$	V
Power Dissipation	$P_{MAX}$			100	mW
Operating Temperature	$T_{OP}$		-20	+70	°C
Storage Temperature	$T_{ST}$		-55	+150	°C

## ELECTRICAL CHARACTERISTICS

Operating Conditions:  $V_{DD} = 1.5V$ , Temperature = 25°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	$V_{DD}$		1.10		3.6	V
Current Consumption	$I_{DD}$	$V_{DD}=1.5V$ , $V_{in}=0\mu V_{rms}$ $V_{DD}=1.5V$ , $V_{in}=20mV_{rms}$ $V_{DD}=3.6V$ , $V_{in}=0\mu V_{rms}$ $V_{DD}=3.6V$ , $V_{in}=20mV_{rms}$	40 24	55 40 58 43	80 65	$\mu A$
Stand-By Current	$I_{DDoff}$				0.1	$\mu A$
Input Frequency Range	$f_{IN}$		40		100	kHz
Minimum Input Voltage	$V_{INmin}$			0.4	1	$\mu V_{rms}$
Maximum Input Voltage	$V_{INmax}$		20			mVrms
Receiver Input Resistance	$R_{RFI}$	$f=40kHz..77.5kHz$		600		k $\Omega$
Receiver Input Capacitance	$C_{RFI}$			0.5		pF
RFI2 Switch On Resistance	$R_{ON2}$	$V_{DD}=1.4V$		5	15	$\Omega$
RFI2 Switch Off Capacitance	$C_{OFF2}$			TBD		pF
Input Levels $ I_{IN}  < 0.5\mu A$	$V_{IL}$ $V_{IH}$		$V_{DD}-0.35$		0.35	V
Output Current $V_{OL} < 0.2V_{DD}$ ; $V_{OH} > 0.8V_{DD}$	$ I_{OUT} $		5			$\mu A$
Output Pulse	$T_{100ms}$	$1\mu V_{rms} \leq V_{IN} \leq 20mV_{rms}$	50		140	ms
	$T_{200ms}$	$1\mu V_{rms} \leq V_{IN} \leq 20mV_{rms}$	150		230	ms
	$T_{500ms}$	$1\mu V_{rms} \leq V_{IN} \leq 20mV_{rms}$	400	500	600	ms
	$T_{800ms}$	$1\mu V_{rms} \leq V_{IN} \leq 20mV_{rms}$	700	800	900	ms
Startup Time	$T_{Start}$	Fast Start-up, $V_{in}=0.4\mu V_{rms}$ Fast Start-up, $V_{in}=20mV_{rms}$		1.3 3.5		s
Output Delay Time	$T_{Delay}$			50	100	ms

**Note:** Stand-by current consumption may increase if  $V_{IH}$  and  $V_{IL}$  differ from  $V_{DD}$  and GND respectively.

TBD = To Be Defined

## FREQUENCY SELECTION

The frequency selection and power down control is accomplished via two digital control pins PDN1 and PDN2. The control logic is presented in table 1.

**Table 1.** Frequency selection and power down control

PDN1	PDN2	RFI2 Switch	Selected Crystal Output	Description
High	High	Open	-	Power down
High	Low	Open	QO1	Frequency 1
Low	High	Closed	QO2	Frequency 2, RFI2 capacitor connected in parallel with antenna
Low	Low	Closed	QO2	Frequency 2, RFI2 capacitor connected in parallel with antenna

The internal antenna tuning capacitor switch (RFI2) and crystal filter output switches (QO1, QO2) are controlled according table 1.

If frequency 1 is selected the RFI2 switch is open and only crystal output QO1 is active. Antenna frequency is determined by antenna inductor  $L_{ANT}$  (see Typical Application on page 5), antenna capacitor  $C_{ANT1}$  and parasitic capacitances related to antenna inputs RFIP, RFIM and RFI2 (see Antenna Tuning Considerations below). Frequency 1 is the highest frequency of the two selected frequencies.

If frequency 2 is selected then RFI2 switch is closed to connect  $C_{ANT2}$  to pin RFIM in parallel with ferrite antenna and tune it to frequency 2. Then only crystal output QO2 is active. Frequency 2 is the lowest frequency of the two selected frequencies.

It is recommended to switch the device to power down for at least 50ms before switching to another frequency. This guarantees fast startup in switching to another frequency. During minimum 50ms power down time the AGC capacitor voltage is completely pulled to VDD and the proper fast startup conditions are met. Without proper fast startup control the startup time can be several minutes. With fast startup it is shortened typically to few seconds.

## ANTENNA TUNING CONSIDERATIONS

The ferrite bar antenna having inductance  $L_{ANT}$  and parasitic coil capacitance  $C_{COIL}$  is tuned to two reception frequencies  $f_1$  and  $f_2$  by parallel capacitors  $C_{ANT1}$  and  $C_{ANT2}$ . The receiver input stage and internal antenna capacitor switches have capacitances  $C_{RFI}$  and  $C_{OFF2}$  which affect the

resonance frequencies.  $C_{OFF2}$  is switch capacitance when switch is open. When the antenna switch is closed the off capacitance is shorted by on resistance of the switch and it is effectively eliminated. Following relationships can be written for the two tuning frequencies.

Frequency  $f_1$  (highest frequency):

$$C_{TOT1} = C_{COIL} + C_{ANT1} + C_{RFI} + C_{OFF2}$$

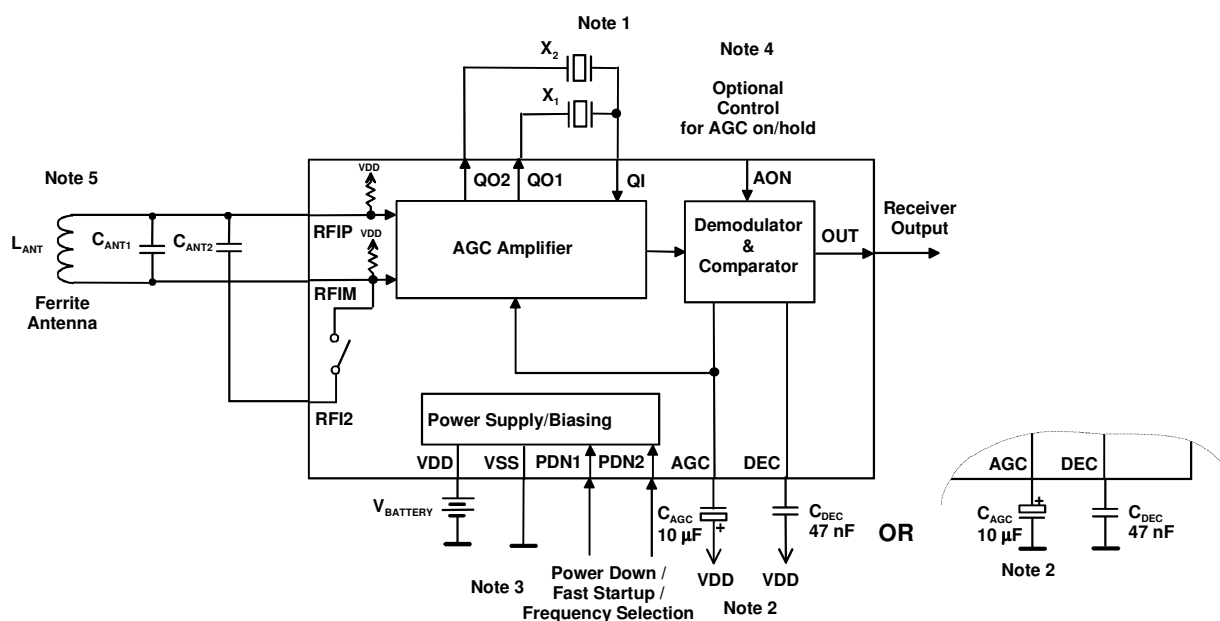
$$f_1 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT1}}}$$

Frequency  $f_2$  (lowest frequency):

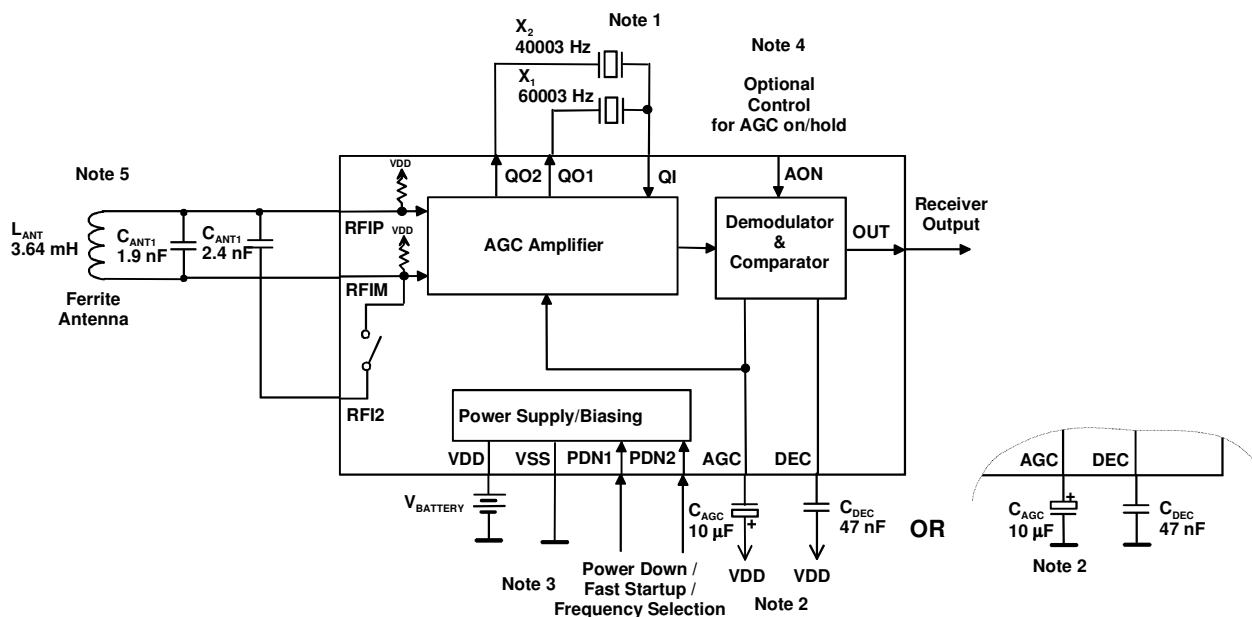
$$C_{TOT2} = C_{COIL} + C_{ANT1} + C_{ANT2} + C_{RFI}$$

$$f_2 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT2}}}$$

## TYPICAL APPLICATION



**Figure 1.** Application circuit of dual band receiver MAS6181



**Figure 2.** Example circuit of dual band receiver MAS6181 for JJY 60 kHz and 40 kHz frequencies

## TYPICAL APPLICATION (Continued)

### Note 1: Crystals

The crystals as well as ferrite antenna frequencies are chosen according to the time signal system (Table 2). The reason why the crystal frequency is about 3 Hz higher than the signal frequency is that the crystal is operated without the loading capacitor. Without loading capacitor the actual resonance frequency is about 3 Hz lower thus 77.503 kHz crystal resonates at 77.500 kHz when no loading capacitor is used.

**Table 2.** Time Signal System Frequencies

Time Signal System	Location	Antenna Frequency	Recommended Crystal Frequency
DCF77	Germany	77.5 kHz	77.503 Hz
HBG	Switzerland	75 kHz	75.003 kHz
MSF	United Kingdom	60 kHz	60.003 kHz
WWVB	USA	60 kHz	60.003 kHz
JJY	Japan	40 kHz and 60 kHz	40.003 kHz and 60.003 kHz
BPC	China	68.5 kHz	68.505 kHz

The crystal shunt capacitance  $C_0$  should be matched as well as possible with the internal shunt capacitance compensation capacitor  $C_c$  of MAS6181. See Compensation Capacitance Options in table 3.

**Table 3.** Compensation Capacitance Options

Device	$C_c$	Crystal Description
MAS6181A1	0.75 pF	For low $C_0$ crystal
MAS6181A2	1.3 pF	For high $C_0$ crystal

It should be noted that grounded crystal package has reduced shunt capacitance. This value is about 85% of floating crystal shunt capacitance. For example crystal with 1pF floating package shunt capacitance can have 0.85pF grounded package shunt capacitance. PCB traces of crystal and external compensation capacitance should be kept at minimum to minimize additional parasitic capacitance which can cause capacitance mismatching.

Highest frequency crystal is connected to crystal output pin 1 (QO1) and the lowest frequency crystal is connected to crystal output pin 2 (QO2). The other pin of each crystal is connected to common crystal input pin QI.

Table 4 below presents some crystal manufacturers having suitable crystals for time signal receiver application.

**Table 4.** Crystal Manufacturers and Crystal Types in Alphabetical Order for Time Signal Receiver Application

Manufacturer	Crystal Type	Dimensions	Web Link
Citizen	CFV-206	ø 2.0 x 6.0	<a href="http://www.citizen.co.jp/tokuhan/quartz/">http://www.citizen.co.jp/tokuhan/quartz/</a>
Epson	C-2-Type	ø 1.5 x 5.0	<a href="http://www.epson.com.co.jp/english/">http://www.epson.com.co.jp/english/</a>
	C-4-Type	ø 2.0 x 6.0	
KDS Daishinku	DT-261	ø 2.0 x 6.0	<a href="http://www.kds.info/index_en.htm">http://www.kds.info/index_en.htm</a>
Microcrystal	MX1V-L2N	ø 2.0 x 6.0	<a href="http://www.microcrystal.com/">http://www.microcrystal.com/</a>
	MX1V-T1K	ø 2.0 x 8.1	
Seiko Instruments	VTC-120	ø 1.2 x 4.7	<a href="http://www.sii-crystal.com">http://www.sii-crystal.com</a>

### Note 2: AGC Capacitor

The AGC and DEC capacitors must have low leakage currents due to very small signal currents through the capacitors. The insulation resistance of these capacitors should be at minimum 100 MΩ. Also probes with at least 100 MΩ impedance should be used for voltage probing of AGC and DEC pins. Electrolytic AGC capacitor should have voltage rating at least 25 V for low enough leakage. DEC capacitor can be low leakage chip capacitor.

## TYPICAL APPLICATION (Continued)

Both the AGC and DEC capacitors can be connected either to VDD or to VSS. To minimize leakage currents during power down the AGC and DEC capacitors are best to be connected to VDD since in power down the AGC and DEC pins go to VDD voltage potential. In this case the positive polarity pin of electrolyte capacitor should be connected to VDD. If the capacitors are connected to VSS then the negative polarity pin of electrolyte capacitor should be connected to VSS.

### Note 3: Power Down / Fast Startup Control

Both power down and fast startup are controlled using the PDN pin. The device is in power down (turned off) if PDN1 = PDN2 = VDD and in power up with other three PDN1 and PDN2 control bit combinations (see table 1 on page 4). Fast startup is triggered automatically when moving from power down to power up. The VDD must have been high before moving from power down to power up to guarantee proper operation of fast startup circuitry. Additionally the device should have been kept in power down state at least 50ms before power up. This guarantees that the AGC capacitor voltage has been completely pulled to VDD during power down. The startup time without proper fast startup control can be several minutes. With fast startup it is shortened typically to few seconds.

### Note 4: Optional Control for AGC On/Hold

AON control pin has internal pull up which turns AGC circuit on all the time if AON pin is left unconnected. Optionally AON control can be used to hold and release AGC circuit. Stepper motor drive of analog clock or watch can produce disturbing amount of noise which can shift the input amplifier gain to unoptimal level. This can be avoided by controlling AGC hold (AON=VSS) during stepper motor drive periods and releasing AGC (AON=VDD) when motors are not driven. The AGC should be in hold only during disturbances and kept on other time released since due to leakage the AGC can change slowly when in hold.

### Note 5: Ferrite Antenna

The ferrite antenna converts the transmitted radio wave into a voltage signal. It has an important role in determining receiver performance. Recommended antenna impedance at resonance is around 150 kΩ.

Low antenna impedance corresponds to low noise but often also to small signal amplitude. On the other hand high antenna impedance corresponds to high noise but also large signal. The optimum performance where signal-to-noise ratio is at maximum is achieved in between.

The antenna should have also some selectivity for rejecting near signal band disturbances. This is determined by the antenna quality factor which should be approximately 100. Much higher quality factor antennas suffer from extensive tuning accuracy requirements and possible tuning drifts by the temperature.

Antenna impedance can be calculated using equation 1 where  $f_0$ ,  $L$ ,  $Q_{ant}$  and  $C$  are resonance frequency, coil inductance, antenna quality factor and antenna tuning capacitor respectively. Antenna quality factor  $Q_{ant}$  is defined by ratio of resonance frequency  $f_0$  and antenna bandwidth  $B$  (equation 2).

$$R_{antenna} = 2\pi \cdot f_0 \cdot L \cdot Q_{antenna} = \frac{Q_{antenna}}{2\pi \cdot f_0 \cdot C} = \frac{1}{2\pi \cdot B \cdot C} \quad \text{Equation 1.}$$

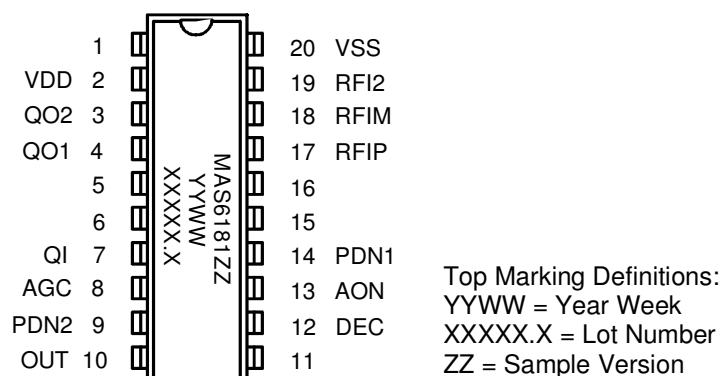
$$Q_{antenna} = \frac{f_0}{B} \quad \text{Equation 2.}$$

Table 5 below presents some antenna manufacturers for time signal application.

**Table 5.** Antenna Manufacturers and Antenna Types in Alphabetical Order for Time Signal Application

Manufacturer	Antenna Type	Dimensions	Web Link
HR Electronic GmbH	60716 (60kHz) 60708 (77.5kHz)	ø 10 x 60 mm	<a href="http://www.hrelectronic.com/">http://www.hrelectronic.com/</a>
Sumida	ACL80A (40kHz)	ø 10 x 80 mm	<a href="http://www.sumida.co.jp/jeita/XJA021.pdf">www.sumida.co.jp/jeita/XJA021.pdf</a>

## MAS6181 SAMPLES IN SBDIL 20 PACKAGE



## PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
	1	NC		
VDD	2	P	Positive Power Supply	
QO2	3	AO	Quartz Filter Output for Crystal 2	
QO1	4	AO	Quartz Filter Output for Crystal 1	
	5	NC		1
	6	NC		1
QI	7	AI	Quartz Filter Input for Crystal	
AGC	8	AO	AGC Capacitor	
PDN2	9	DI	Power Down/Frequency Selection Input 2	2
OUT	10	DO	Receiver Output	3
	11	NC		
DEC	12	AO	Demodulator Capacitor	
AON	13	DI	AGC On Control	4
PDN1	14	DI	Power Down/Frequency Selection Input 1	2
	15	NC		
	16	NC		
RFIP	17	AI	Positive Receiver Input	5
RFIM	18	AI	Negative Receiver Input	5
RFI2	19	AI	Receiver Input 2 (for Antenna Capacitor 2)	
VSS	20	G	Power Supply Ground	

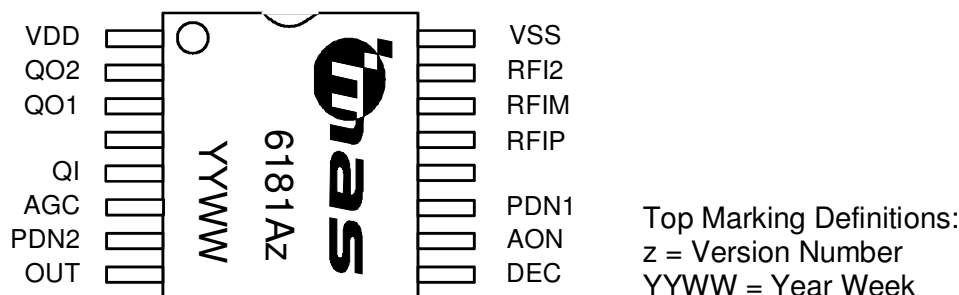
A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

### Notes:

- Pins 5 and 6 between QO1 and QI must be connected to VSS to eliminate DIL package lead frame parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
- PDN1 = PDN2 = VDD means receiver off
  - Fast start-up is triggered when the receiver is after power down controlled to power up
- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
  - the output is a current source/sink with  $|I_{OUT}| > 5 \mu A$
  - at power down the output is pulled to VSS (pull down switch)
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
  - Internal pull-up with current  $< 1 \mu A$  which is switched off at power down
- Receiver inputs RFIP and RFIM have both 600 k $\Omega$  biasing resistors towards VDD.



## PIN CONFIGURATION & TOP MARKING FOR PLASTIC TSSOP-16 PACKAGE



## PIN DESCRIPTION

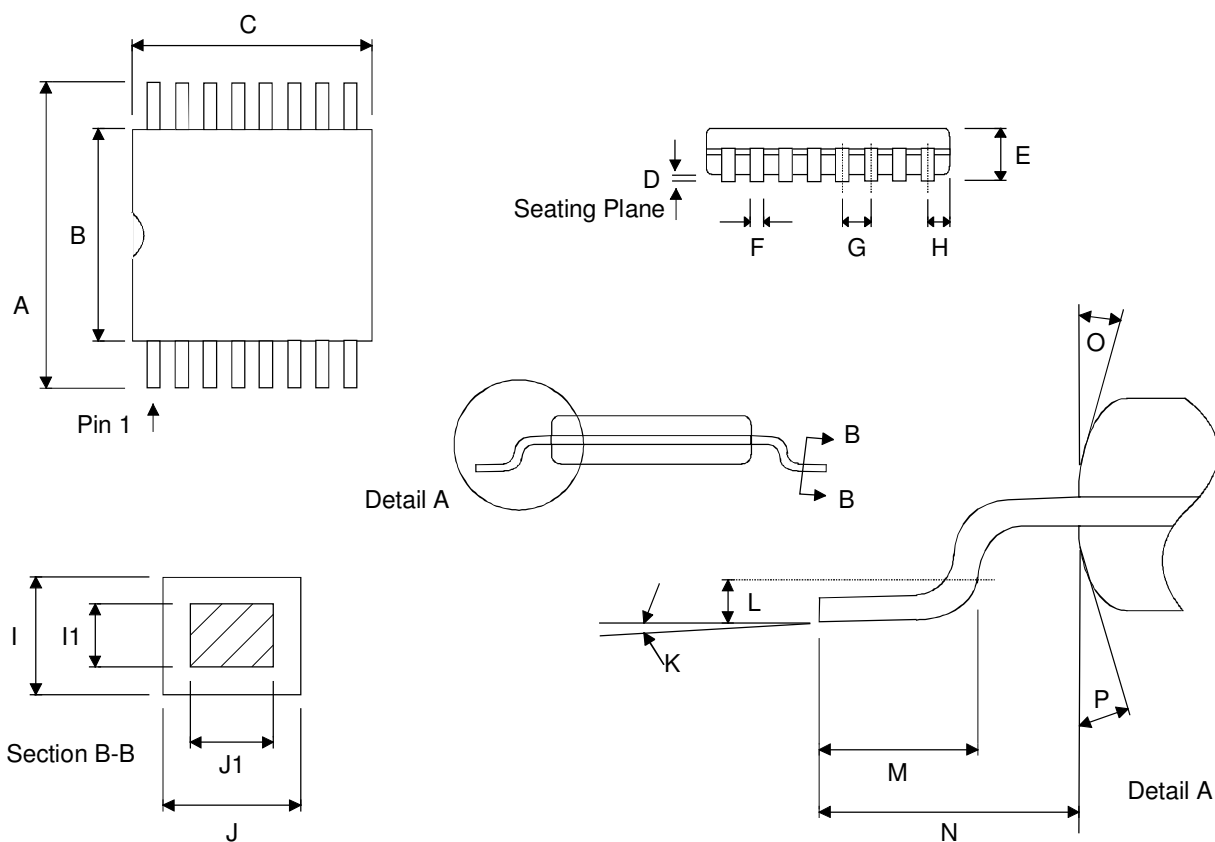
Pin Name	Pin	Type	Function	Note
VDD	1	P	Positive Power Supply	
QO2	2	AO	Quartz Filter Output for Crystal 2	
QO1	3	AO	Quartz Filter Output for Crystal 1	
	4	NC		1
QI	5	AI	Quartz Filter Input for Crystal and External Compensation Capacitor	
AGC	6	AO	AGC Capacitor	
PDN2	7	DI	Power Down/Frequency Selection Input 2	2
OUT	8	DO	Receiver Output	3
DEC	9	AO	Demodulator Capacitor	
AON	10	DI	AGC On Control	4
PDN1	11	DI	Power Down/Frequency Selection Input 1	2
	12	NC		
RFIP	13	AI	Positive Receiver Input	5
RFIM	14	AI	Negative Receiver Input	5
RFI2	15	AI	Receiver Input 2 (for Antenna Capacitor 2)	
VSS	16	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

### Notes:

- Pin 4 between QO1 and QI must be connected to VSS to eliminate TSSOP package lead frame parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
- PDN1 = PDN2 = VDD means receiver off
  - Fast start-up is triggered when the receiver is after power down controlled to power up
- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
  - the output is a current source/sink with  $|I_{OUT}| > 5 \mu A$
  - at power down the output is pulled to VSS (pull down switch)
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
  - Internal pull-up with current  $< 1 \mu A$  which is switched off at power down
- Receiver inputs RFIP and RFIM have both 600 k $\Omega$  biasing resistors towards VDD.

## PACKAGE (TSSOP-16) OUTLINES



Dimension	Min	Max	Unit
A	6.40 BSC		mm
B	4.30	4.50	mm
C	5.00 BSC		mm
D	0.05	0.15	mm
E		1.10	mm
F	0.19	0.30	mm
G	0.65 BSC		mm
H	0.18	0.28	mm
I	0.09	0.20	mm
I1	0.09	0.16	mm
J	0.19	0.30	mm
J1	0.19	0.25	mm
K	0°	8°	
L	0.24	0.26	mm
M	0.50	0.75	mm
(The length of a terminal for soldering to a substrate)			
N	1.00 REF		mm
O	12°		
P	12°		

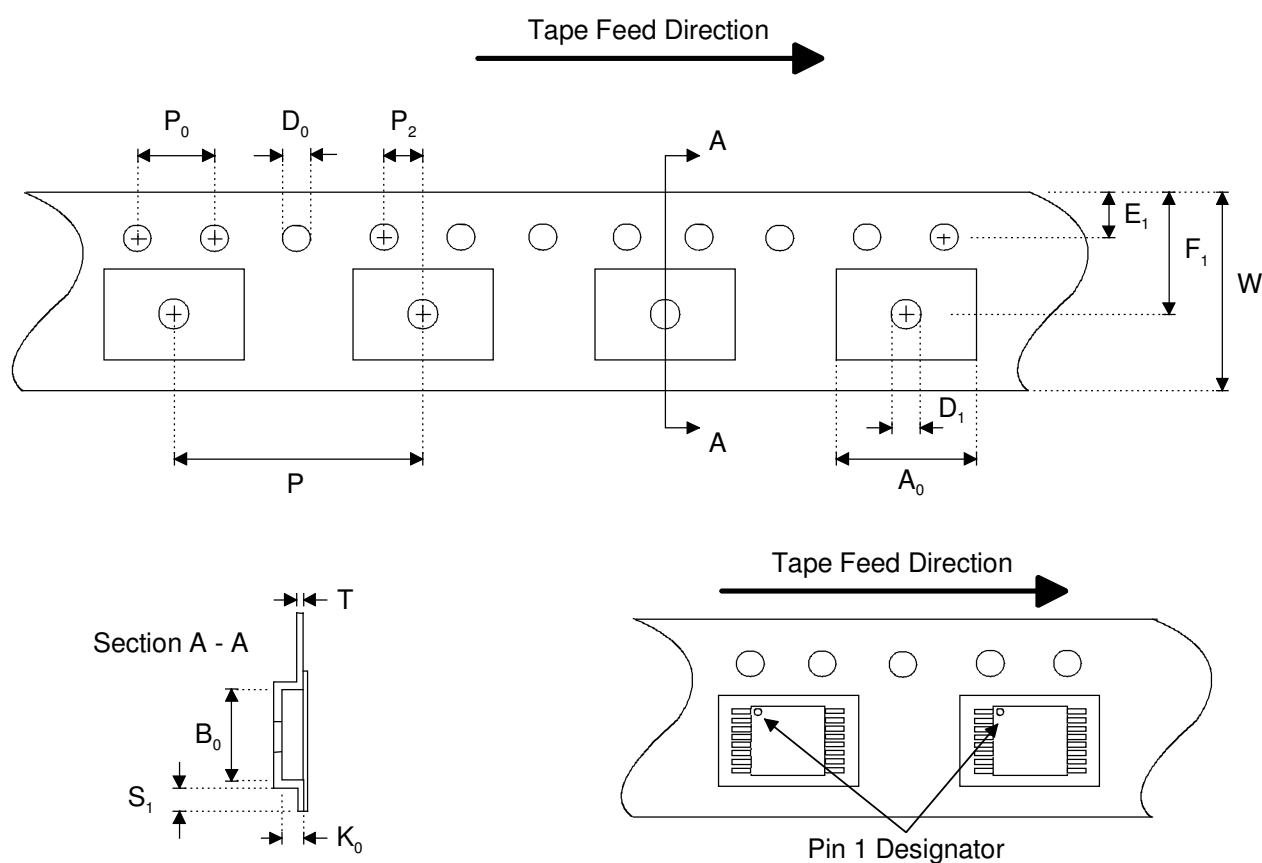
Dimensions do not include mold flash, protrusions, or gate burrs.  
All dimensions are in accordance with JEDEC standard MO-153.

## SOLDERING INFORMATION

### ◆ For Pb-Free, RoHS Compliant TSSOP-16

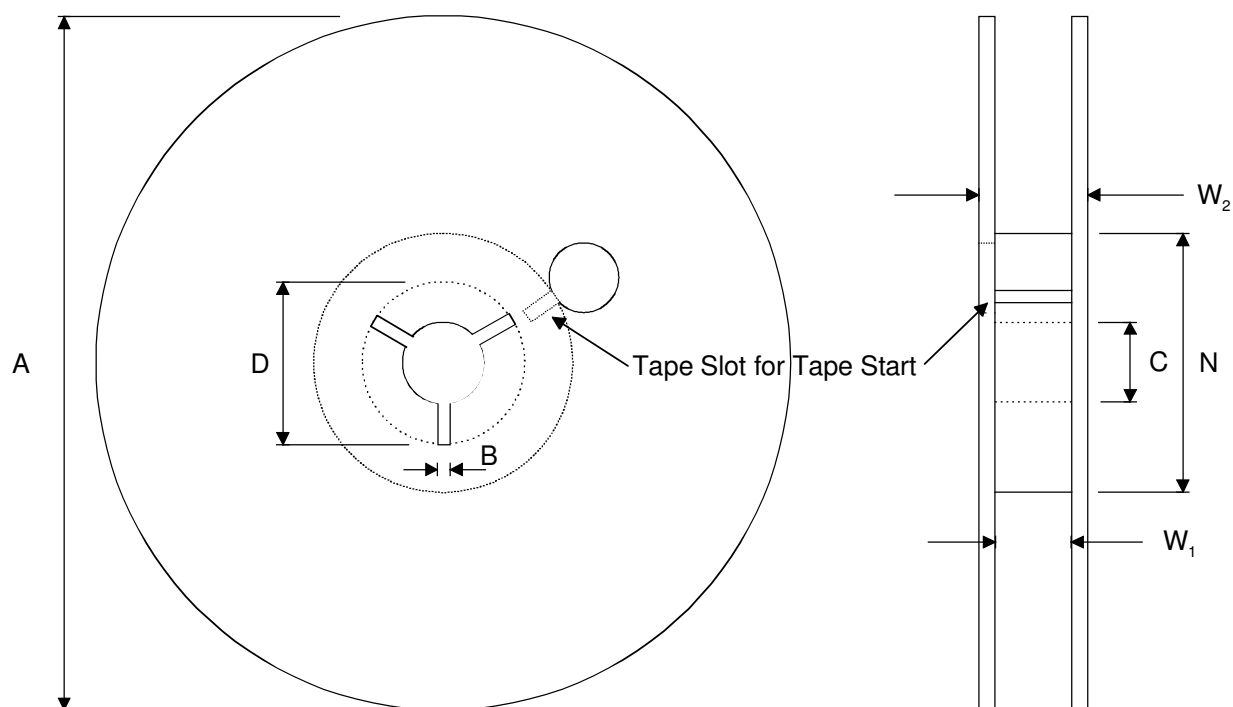
Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. <a href="http://www.jedec.org">http://www.jedec.org</a>
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

## EMBOSED TAPE SPECIFICATIONS



Dimension	Min	Max	Unit
$A_0$	6.50	6.70	mm
$B_0$	5.20	5.40	mm
$D_0$	1.50 +0.10 / -0.00		mm
$D_1$	1.50		mm
$E_1$	1.65	1.85	mm
$F_1$	7.20	7.30	mm
$K_0$	1.20	1.40	mm
$P$	11.90	12.10	mm
$P_0$	4.0		mm
$P_2$	1.95	2.05	mm
$S_1$	0.6		mm
$T$	0.25	0.35	mm
$W$	11.70	12.30	mm

## REEL SPECIFICATIONS

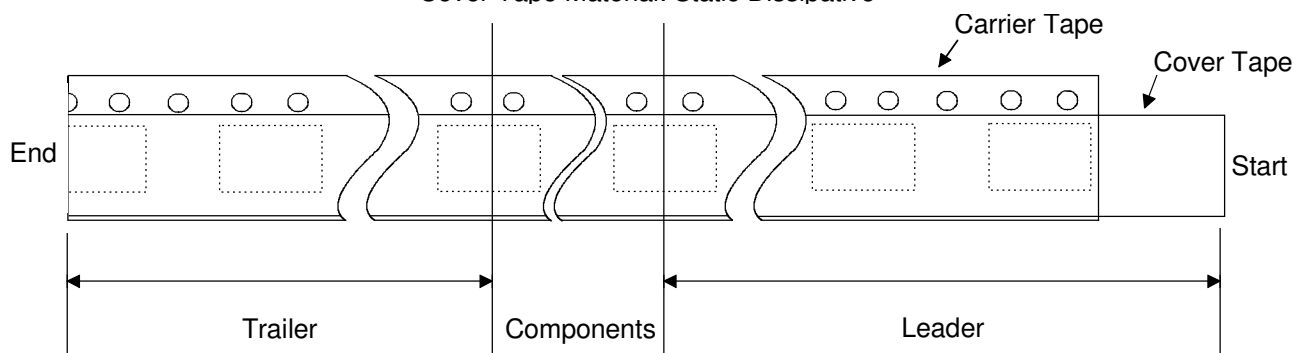


2000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative

Carrier Tape Material: Conductive

Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W <sub>1</sub> (measured at hub)	12.4	14.4	mm
W <sub>2</sub> (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

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**ORDERING INFORMATION**

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Product Code	Product	Description	Capacitance Option
MAS6181A1TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 $\mu\text{m}$ .	$C_C = 0.75 \text{ pF}$
MAS6181A2TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 $\mu\text{m}$ .	$C_C = 1.3 \text{ pF}$
MAS6181A1UC06	Dual Band AM-Receiver IC with Differential Input	TSSOP-16, Pb-free, RoHS compliant, Tape & Reel	$C_C = 0.75 \text{ pF}$

Contact Micro Analog Systems Oy for other wafer thickness options.

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**MICRO ANALOG SYSTEMS OY CONTACTS**

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Micro Analog Systems Oy Kamreerintie 2, P.O. Box 51 FIN-02771 Espoo, FINLAND	Tel. +358 9 80 521 Fax +358 9 805 3213 <a href="http://www.mas-oy.com">http://www.mas-oy.com</a>
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