CML Microcircuits

COMMUNICATION SEMICONDUCTORS

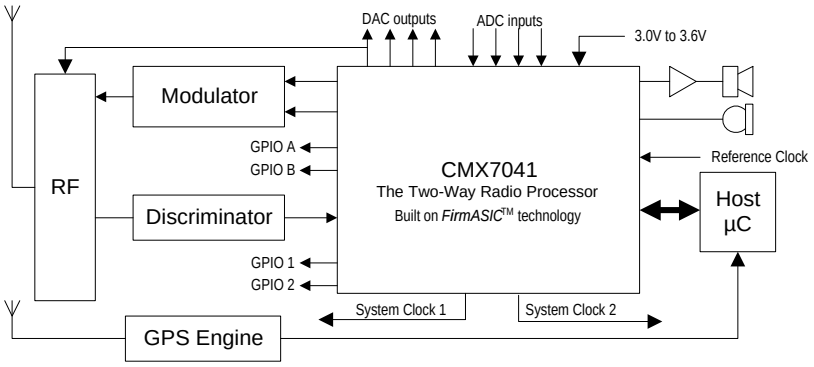
CMX7041
The Two-Way Radio Processor

D/7041/1 February 2006 **DATASHEET** Provisional Issue

CMX7041: Baseband Audio and Data Processor with System Clock O/P for Use in Analogue Radio Systems

Features

- **Concurrent Audio/Signalling/Data operations**
- **Full Audio-band Processing: Pre and De-emphasis, Compandor, Scrambler and Selectable 2.55 / 3 kHz Filters**
- **Inband Signalling: Selcall and DTMF**
- **2 x Auxiliary ADCs and 4 x Auxiliary DACs**
- **Low-power (3.0V to 3.6V) Operation**
- **C-BUS Serial Interface to Host µController**
- **3 x Analogue Inputs (Mic or Discriminator)**
- **FFSK/MSK Data Modem with Packet or Free-format modes with FEC, CRC, Interleaving and Scrambling**
- **Sub-Audio Signalling: CTCSS, DCS**
- **Auxiliary System Clock Outputs**
- **Tx Outputs for Single or Two Point Modulation**
- **Available in 48-pin LQFP and VQFN Packages**
- **Flexible Powersave Modes**



Brief Description

The CMX7041 is a full-function, half-duplex, audio, signalling and data processor IC. This makes it a suitable device for both the leisure radio markets (FRS, MURS, PMR446 and GMRS) and for professional radio products (PMR/LMR and Trunking) with or without signalling and data facilities.

The device utilises CML's proprietary *FirmASIC*™ component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external EEPROM or from a host µController over the built-in C-BUS serial interface. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

The CMX7041 features two programmable system clocks to minimise chip count in the final application.

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The device performs simultaneous processing of subaudio and inband signalling and audio-band processing (including frequency inversion scrambling, companding and pre- or de-emphasis). Other features include a complete FFSK/MSK modem for packetised or free-format data, two Auxilliary ADC channels with four selectable inputs and up to four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping).

The device has flexible powersaving modes and is available in both LQFP and VQFN packages.

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

This datasheet is the first part of a two-part document: the User Manual can be obtained by registering your interest on the CML website [www.cmlmicro.com].

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It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

1 Block Diagram

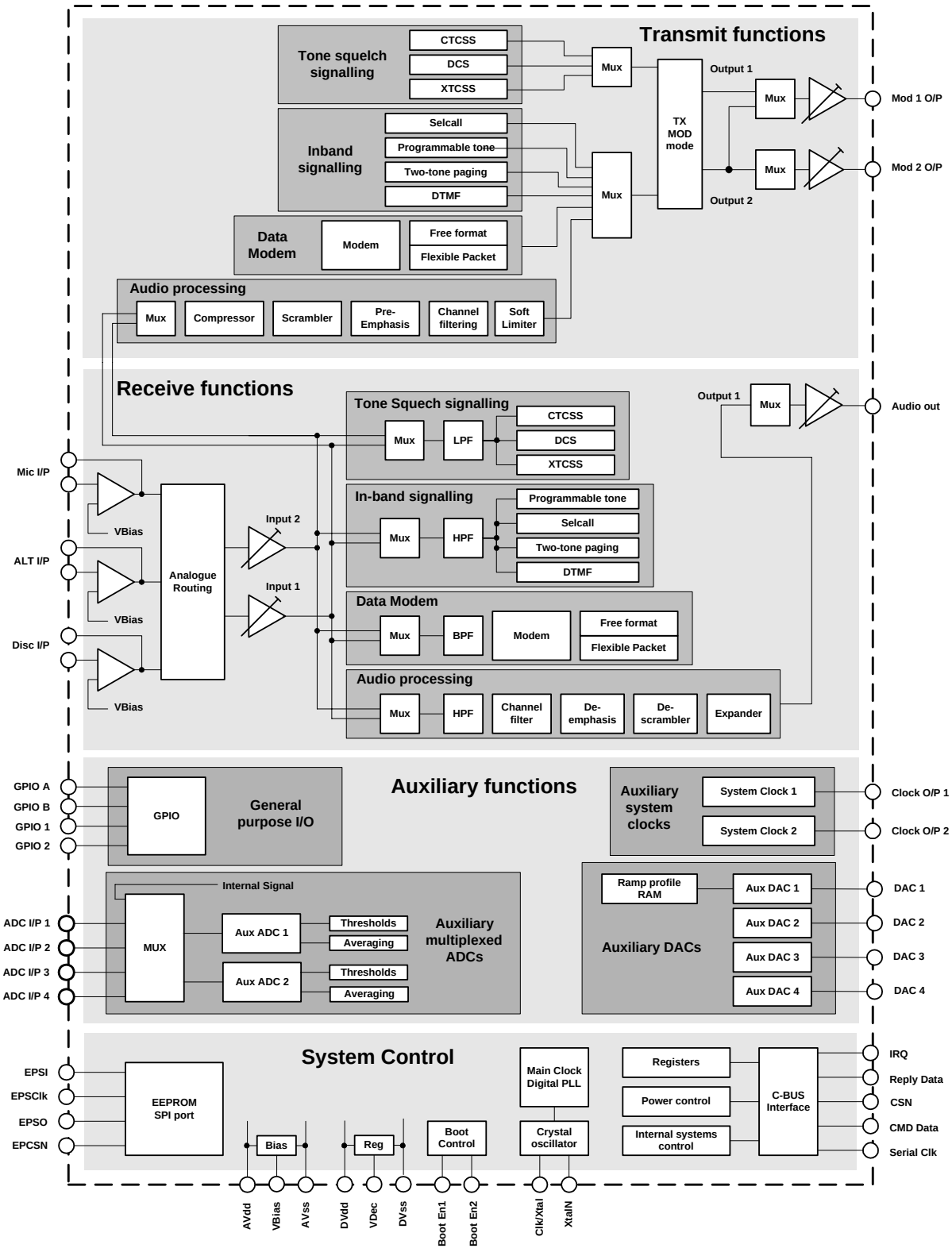


Figure 1 Block Diagram

2 Signal List

48-pin (Q3 / L4) Pin No.	Signal Name	Type	Description
1	EPSI	OP	EEPROM Serial Interface: SPI bus Output.
2	EPSCLK	OP	EEPROM Serial Interface: SPI bus Clock.
3	EPSO	IP+PD	EEPROM Serial Interface: SPI bus Input.
4	EPSCSN	OP	EEPROM Serial Interface: SPI bus ChipSelect.
5	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program.
6	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program.
7	DVss	PWR	Negative supply rail (ground) for the digital on-chip circuits.
8	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to VSS(D) when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
9	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DVss by capacitors mounted close to the device pins. No other connections allowed. If the device is to be run from a 2.5V external supply, then VDEC must be connected directly to DVdd pin.
10	GPIO 1	BI	General Purpose I/O pin – leave unconnected.
11	GPIO A	BI	General Purpose I/O pin – leave unconnected.
12	GPIO B	BI	General Purpose I/O pin – leave unconnected.
13	SYS CLOCK 1	OP	Synthesised Digital System Clock Output 1.
14	DVss	PWR	The negative supply rail (ground) for the digital on-chip circuits.
15	GPIO 2	BI	General Purpose I/O pin – leave unconnected.
16	DISC	IP	Channel 1 inverting input.
17	DISCFB	OP	Channel 1 input amplifier feedback.
18	ALT	IP	Channel 2 inverting input.
19	ALTFB	OP	Channel 2 input amplifier feedback.
20	MICFB	OP	Channel 3 input amplifier feedback.
21	MIC	IP	Channel 3 inverting input.
22	AVss	PWR	The negative supply rail (ground) for the analogue on-chip circuits.
23	MOD1	OP	Modulator 1 output.
24	MOD2	OP	Modulator 2 output.
25	V_{BIAS}	OP	Internally generated bias voltage of about AVdd/2, except when the device is in 'Powersave' mode when VBIAS will discharge to AVss. Must be decoupled to AVss by a capacitor mounted close to the device pins. No other connections allowed.
26	AUDIOOUT	OP	Audio output.
27	AUXADC1	IP	Auxiliary ADC input 1.

48-pin (Q3 / L4) Pin No.	Signal Name	Type	Description
28	AUXADC2	IP	Auxiliary ADC input 2.
29	AUXADC3	IP	Auxiliary ADC input 3.
30	AUXADC4	IP	Auxiliary ADC input 4.
31	AVdd	PWR	Positive 3.3V supply rail for the analogue on-chip circuits. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVss by capacitors mounted close to the device pins.
32	AUXDAC1	OP	Auxiliary DAC output 1 / RAMDAC.
33	AUXDAC2	OP	Auxiliary DAC output 2.
34	AVss	PWR	Negative supply rail (ground) for the analogue on-chip circuits.
35	AUXDAC3	OP	Auxiliary DAC output 3.
36	AUXDAC4	OP	Auxiliary DAC output 4.
37	DVss	PWR	Negative supply rail (ground) for the digital on-chip circuits.
38	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DVss by capacitors mounted close to the device pins. No other connections allowed. If the device is to be run from a 2.5V external supply, then VDEC must be connected directly to DVdd pin.
39	XTAL/CLOCK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source.
40	XTALN	OP	The output of the on-chip Xtal oscillator inverter.
41	DVdd	PWR	The 3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVss by capacitors mounted close to the device pins.
42	COMMAND DATA	IP	C-BUS: Serial data input from the µC.
43	REPLY DATA	TS OP	C-BUS: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
44	-	NC	Reserved – do not connect this pin.
45	DVss	PWR	Negative supply rail (ground) for the digital on-chip circuits.
46	SERIAL CLOCK	IP	C-BUS: The C-BUS serial clock input from the µC.
47	SYS CLOCK 2	OP	Synthesised Digital System Clock Output 2.
48	CSN	IP	C-BUS: The C-BUS chip select input from the µC - there is no internal pullup on this input.

Notes:
IP = Input (+ PU/PD = internal pullup / pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

3 External Components

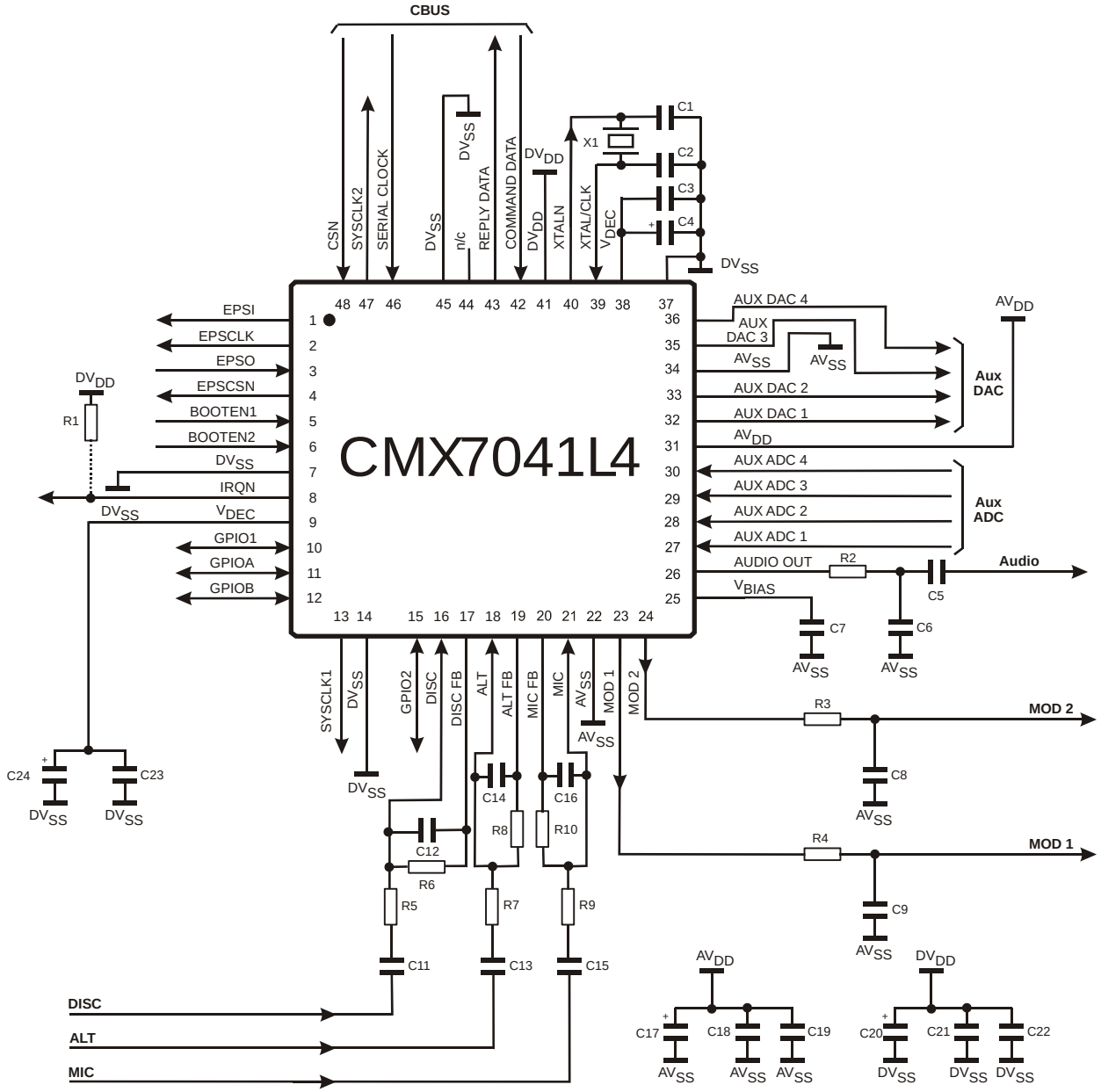


Figure 2 CMX7041 Recommended External Components

R1	100kΩ	C1	18pF	C11	See note 5	C21	10nF
R2	100kΩ	C2	18pF	C12	100pF	C22	10nF
R3	100kΩ	C3	10nF	C13	See note 5	C23	10µF
R4	100kΩ	C4	10µF	C14	100pF	C24	10nF
R5	See note 2	C5	1nF	C15	See note 5	C25	10nF
R6	100kΩ	C6	100pF	C16	200pF	C26	10µF
R7	See note 3	C7	100nF	C17	10µF		
R8	100kΩ	C8	100pF	C18	10nF	X1	6.144MHz
R9	See note 4	C9	100pF	C19	10nF		See note 1
R10	100kΩ	C10	*not used*	C20	10µF		

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 6.144MHz crystal is assumed, other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain (assuming C11 is not present) of the discriminator input, as follows:

$$|GAIN_{Disc}| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the DISCFB pin is within the discriminator input signal range specified in 6.14.2.

3. R7 should be selected to provide the desired dc gain (assuming C13 is not present) of the alternative input as follows:

$$|GAIN_{Alt}| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the ALTFB pin is within the alternative input signal range specified in 6.13.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the microphone input as follows:

$$|GAIN_{Mic}| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 6.14.1.

5. C11, C13 and C15 should be selected to maintain the lower frequency roll-off of the microphone, alternative and discriminator inputs as follows:

$$C11 \geq 1.0\mu F \times |GAIN_{Disc}|$$
$$C13 \geq 1.0\mu F \times |GAIN_{Alt}|$$
$$C15 \geq 30nF \times |GAIN_{Mic}|$$

6. ALT and ALTFB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to Avss.

4 PCB Layout Guidelines and Power Supply Decoupling

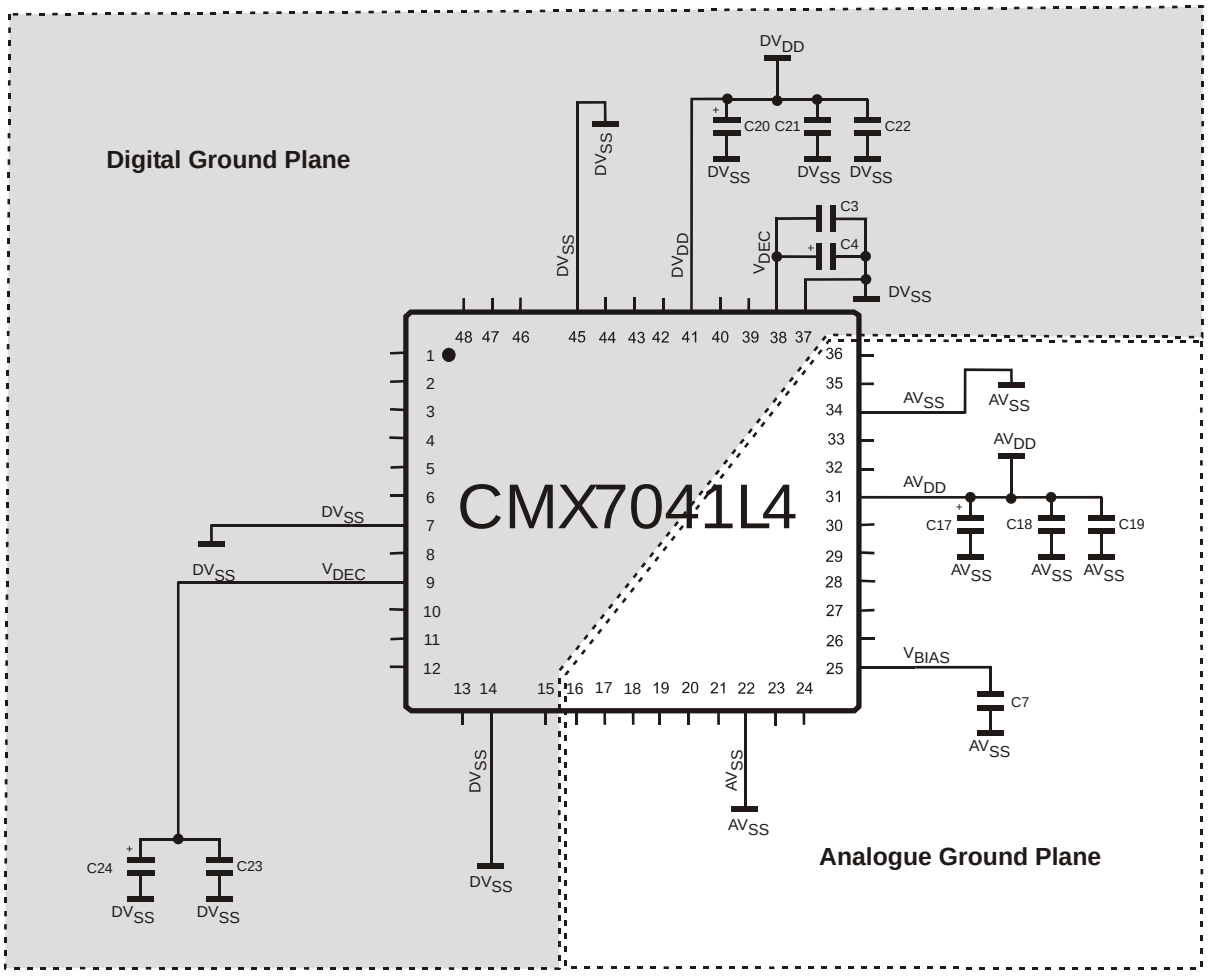


Figure 3 CMX7041 Power Supply Connections and De-coupling

Component Values as per Figure 2.

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7041 and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22, C24 and C25 should be as close as possible to the CMX7041. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX7041, with provision to make links between them, close to the CMX7041. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers. It is recommended that no connection be made to the central metal pad on Q3 packages.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The single ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal X1 may be replaced with an external clock source.

5 General Description

The CMX7041 is intended for use in half duplex analogue two way mobile radio or family radio equipment and is particularly suited to both the PMR market and enhanced MURS / GMRS / FRS with GPS terminal designs. The CMX7041 provides radio signal encoder and decoder functions for: Audio, In-band tones, XTCSS, CTCSS, DCS and FFSK/MSK data, permitting simple to sophisticated levels of tone control and data transfer. A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The CMX7041 includes a crystal clock generator, with buffered output, to provide a common system clock if required. A block diagram of the CMX7041 is shown in Figure 1.

The signal processing blocks can be individually assigned to either of two signal processing paths, which in turn, can be routed from any of the three audio / discriminator input pins. This allows for a very flexible routing architecture and allows the facility for different processing blocks to act on different analogue inputs. Eg: CTCSS may be processed from the DISC input, while Selcall can be processed from the ALT input in parallel.

Tx functions:

Audio

- Single/dual microphone inputs with input amplifier and programmable gain adjustment
- Filtering selectable for 12.5kHz and 25kHz channels
- Selectable pre-emphasis
- Selectable compression
- Selectable frequency inversion voice scrambling
- 2-point modulation outputs with programmable level adjustment

Signalling

- Pre-programmed 51 tone CTCSS encoder
- 120 / 180 degree CTCSS phase shift generation
- Programmable 23/24bit DCS encoder
- Programmable Selcall generator
- Programmable audio tone generator (for custom audio tones)
- Programmable DTMF generator
- Pre-programmed XTCSS and in-band tone encoder
- 1200/2400 baud MSK data packet encoder (suitable for text messaging/paging, caller identification, caller location, digital poll of remote radio location, GPS information in NMEA 0183 format, data transfer, MPT1327 etc.) incorporating interleaving, FEC, CRC and data scrambler

Rx functions:

Audio

- Single/dual demodulator inputs with input amplifier and programmable gain adjustment
- Audio-band and sub-audio rejection filtering
- Selectable de-emphasis
- Selectable expansion
- Selectable frequency inversion voice de-scrambling
- Software volume control

Signalling

- 1 from 51 CTCSS decoder + Tone Clone™ mode
- 120 / 180 degree CTCSS phase shift detection
- 23/24bit DCS decoder
- Programmable Selcall decoder
- Pre-programmed in-band tone decode with XTCSS 4-tone addressing
- 1200/2400 baud MSK data packet decoder with automatic bit rate recognition, 16 bit frame sync detector, error correction, data de-scrambler and packet disassembly
- NWR SAME and WAT detector

Auxiliary Functions:

- 2 programmable system clock outputs

- 2 auxiliary ADCs with four selectable input paths
- 4 auxiliary DACs, one with built-in programmable RAMDAC

Interface:

- C-BUS, 4 wire high speed synchronous serial command / data bus
- Open drain IRQ to host
- Four GPIO pins
- EEPROM boot mode
- C-BUS boot mode

6 Detailed Descriptions

6.1 Xtal Frequency

The CMX7041 is designed to work with a Xtal or external frequency source of 6.144MHz. If this default configuration is not used, then Program Register Block 3 needs to be loaded with the correct values to ensure that the device will work to specification with the user specified clock frequency. A table of common values can be found in Table 1. Note the maximum Xtal frequency is 12.288MHz, although an external clock source of up to 24MHz can be used.

The register values in Table 1 are shown in hex, the default settings are shown in bold, and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new P3.2-3 settings take effect following the write to P3.3 (the settings in P3.4-7 are implemented on a change to Rx or Tx mode).

Table 1 Xtal/clock frequency settings for Program Block 3

Program Register			External frequency source (MHz)							
			3.579	**6.144**	9.0592	12.0	12.8	16.368	16.8	19.2
P3.2	Idle	GP Timer	*$0017*	**$0018**	*$0018*	$0019	$0019	*$0018*	$0019	$0018
P3.3		VCO output and AUX clk divide	*$0085*	**$0088**	*$010F*	*$010F*	*$0110*	*$0095*	*$0115*	$0099
P3.4	Rx or Tx	Ref clk divide	*$0043*	**$0040**	$00C6	$007D	$00C8	$0155	$015E	$00C8
P3.5		PLL clk divide	*$0398*	**$0200**	$0370	$0200	$0300	$0400	$0400	$0200
P3.6		VCO output and AUX clk divide	*$0140*	**$0140**	$0140	$0140	$0140	$0140	$0140	$0140
P3.7		Internal ADC / DAC clk divide	*$0808*	**$0808**	$0808	$0808	$0808	$0808	$0808	$0808

6.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7041 and the host µC; this interface is compatible with microwire, SPI, etc. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 6.15.1.

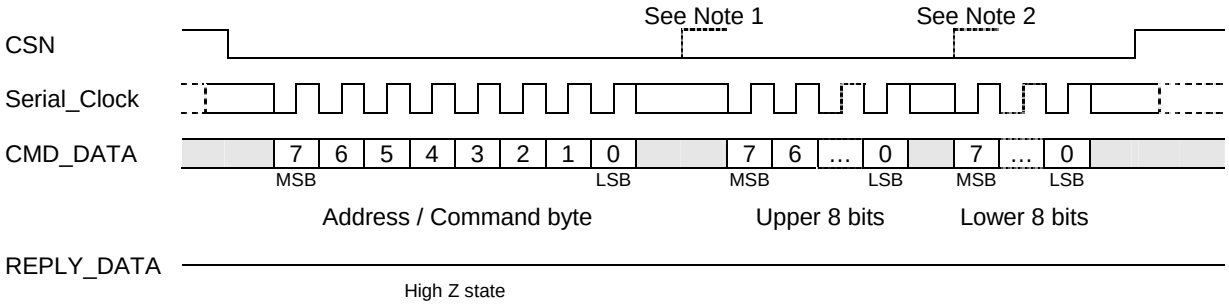
6.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7041's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single Address byte sent from the µC which may be followed by one or more Data byte(s) sent from the µC to be written into one of the CMX7041's Write Only Registers, or one or more data byte(s) read out from one of the CMX7041's Read Only Registers, as illustrated in Figure 4.

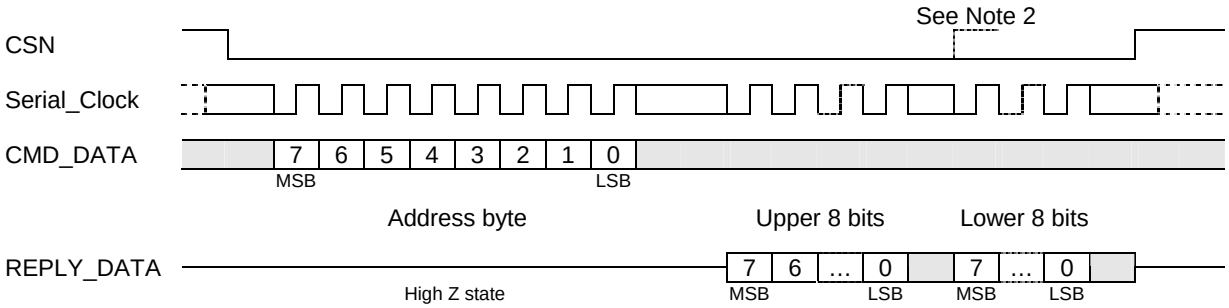
Data sent from the µC on the Command Data line is clocked into the CMX7041 on the rising edge of the Serial Clock input. Reply Data sent from the CMX7041 to the µC is valid when the Serial Clock is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an Address byte is dependent on the value of the Address byte. The most significant bit of the address or data are sent first. For detailed timings see section 7.2.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 4 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CMD_DATA and REPLY_DATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The Serial_Clock input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CMD_DATA and REPLY_DATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

6.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML website, following registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external EEPROM. The maximum possible size of Function Image™ is 46 kbytes, although a typical FI will be much less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7041 until the next power-on or C-BUS General Reset.

Once the FI has been loaded, the CMX7041 will report back a pair of checksum values in the C-BUS registers $A9, $AA and $B8, $B9 and its product identification code, $7041, in C-BUS register $C5. The checksums can be verified against the published values to ensure that the FI has loaded correctly. The host should then write the 32-bit Device Activation Code to C-BUS register $C8 to enable the FI to execute. Once the FI has been activated, the checksum and product identification values are no longer available.

Both the Device Activation Code and the checksum values are available from the CML website.

Table 2 BOOTEN pin states

	BOOTEN2	BOOTEN1
C-BUS Host load	1	1
reserved	1	0
EEPROM load	0	1
No FI load	0	0

Note: In the event that a General Reset needs to be issued without the requirement to re-load the FI, the BOOTEN pins must both be cleared to '0' before issuing the Reset command. The Checksum values will be reported and the Device Activation code will need to be sent in a similar manner as that shown in Figure 6. There will not be any FI loading delay.

6.3.1 FI loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7041 at power-on over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration, the CMX7041 powered up and placed into Program Mode, the data can then be sent directly over the C-BUS to the CMX7041.

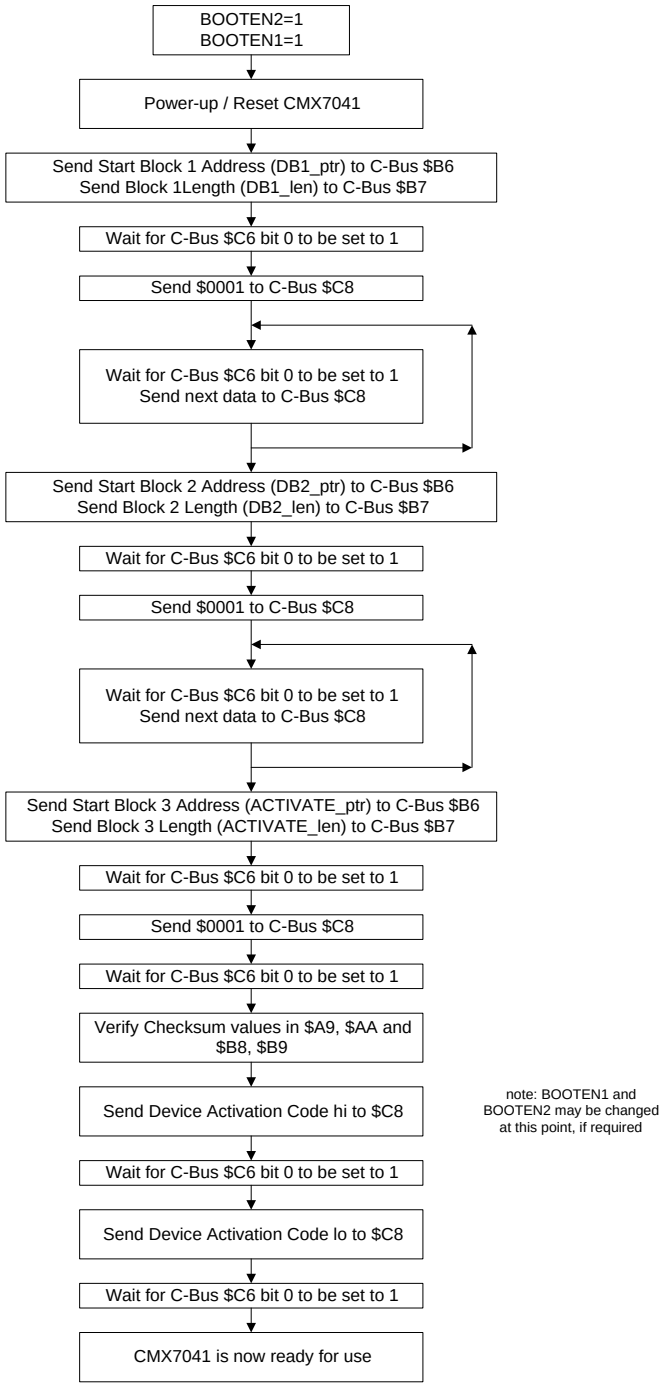


Figure 5 FI loading from Host

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

6.3.2 FI loading from EEPROM

The FI must be converted into a format for the EEPROM programmer (normally Intel Hex) and loaded into the EEPROM either by the host or an external programmer. The CMX7041 needs to have the BOOTEN pins set to EEPROM load, and then on power-on, or following a C-BUS General Reset, the CMX7041 will automatically load the data from the EEPROM without intervention from the host controller.

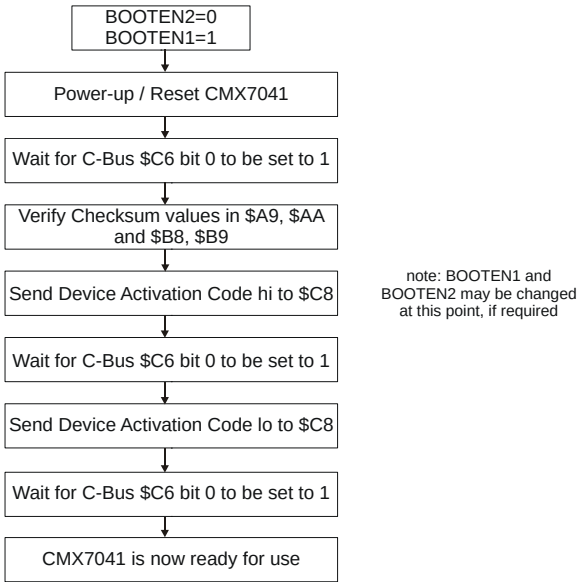


Figure 6 FI loading from EEPROM

The CMX7041 has been designed to function with Atmel AT25HP512 devices, however other manufacturers parts may also be suitable. The time taken to load the FI is dependant on the Xtal frequency, with a 6.144MHz Xtal, it should load in less than 1 second.

6.4 Device Control

The CMX7041 can be set into many modes to suit the environment in which it is to be used. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation, enable the relevant hardware sections via the Power Down Control register, set the appropriate mode registers to the desired state (Audio, Inband, Sub-Audio, Data etc.), select the required Signal Routing, and then use the Mode Control register to place the device into Rx or Tx mode. To conserve power when the device is not actively processing an analogue signal, place the device into Idle mode. Additional Powersaving can be achieved by disabling the unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled.

See:

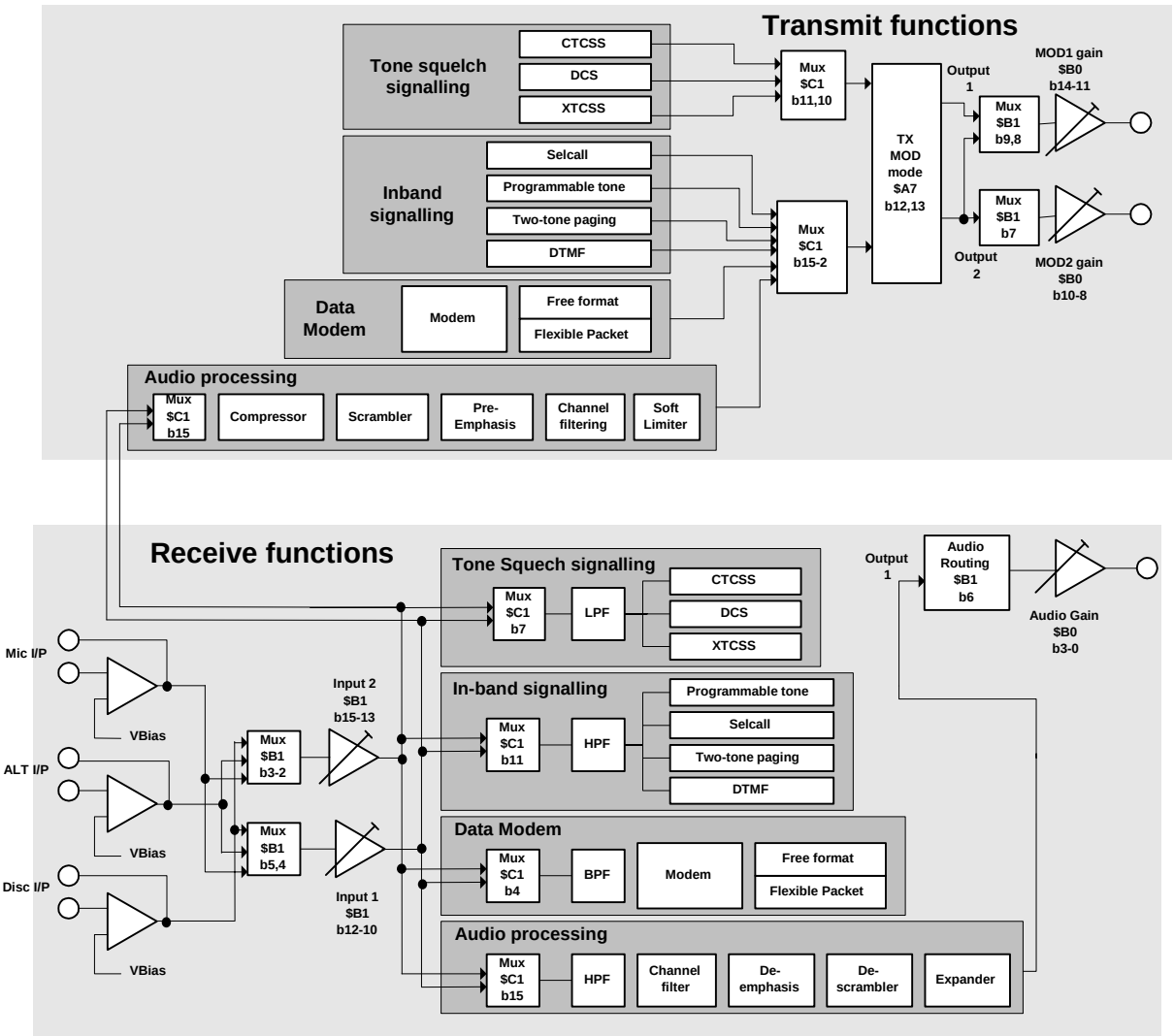
- Power Down Control - $C0 write
- Mode Control – $C1 write

6.4.1 Signal Routing

The CMX7041 offers a very flexible routing architecture, with three signal inputs, two separate signal processing paths and a selection of two modulator outputs (to suit 2-point modulation schemes) and a single Audio output. Each of the signal processing blocks can be independently routed to either of the Input blocks, which can be routed to any of the three input signal pins. The outputs from signal processing blocks are determined by the settings of the AuxADC and TX MOD mode register in Tx mode.

See:

- Input Gain and Output Signal Routing - $B1 write
- AuxADC and TX MOD mode - $A7 write
- Mode Control – $C1 write



The analogue gain / attenuation of each input and output can be set individually, with additional Fine Gain control available via the Programming registers.

See:

- Analogue Output Gain - $B0 write
- Input Gain and Output Signal Routing - $B1 write

6.4.2 Mode Control

The CMX7041 operates in one of three modes:

- o IDLE
- o Rx
- o Tx

At power-on or following a Reset, the device will automatically enter IDLE mode, which allows for the maximum powersaving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled).
It is only possible to write to the Programming register whilst in IDLE mode.

See:

- o Mode Control – $C1 write

6.5 Audio Functions

The audio signal can be processed in several ways, depending on the implementation required, by selecting the relevant bits in the Audio Control – $C2 write register. In both Rx and Tx, a selectable channel filter to suit either the 12.5kHz or 25kHz TIA channel mask can be selected. This filter also incorporates a soft limiter to reduce the effects of over-modulation. Other features include 300Hz HPF, pre- and de-emphasis, companding and frequency inversion scrambling, all of which may be individually enabled.

6.5.1 Audio Receive Mode

The CMX7041 operates in half duplex, so whilst in receive mode the transmit path (microphone input and modulator output amplifiers) can be disabled and powered down if required. The AUDIO output signal level is equalised (to V_{BIAS}) before switching between the audio port and the modulator ports, to minimise unwanted audible transients. The Off/Powersave level of the modulator outputs is the same as the V_{BIAS} pin, so the audio output level must also be at this level before switching.

See:

- o Audio Control – $C2 write

Receiving Audio Band Signals

When a voice-based signal is being received, it is up to the µC, in response to signal status information provided by the CMX7041, to control muting/enabling of the audio signal to the AUDIO output.

The discriminator path through the device has a programmable gain stage. Whilst in receive mode this should normally be set to 0dB (the default) gain.

Receive Filtering

The incoming signal is filtered, as shown in Figure 7 (with the 300Hz HPF also active), to remove sub-audio components and to minimise high frequency noise. When appropriate, the audio signal can then be routed to the AUDIO output.

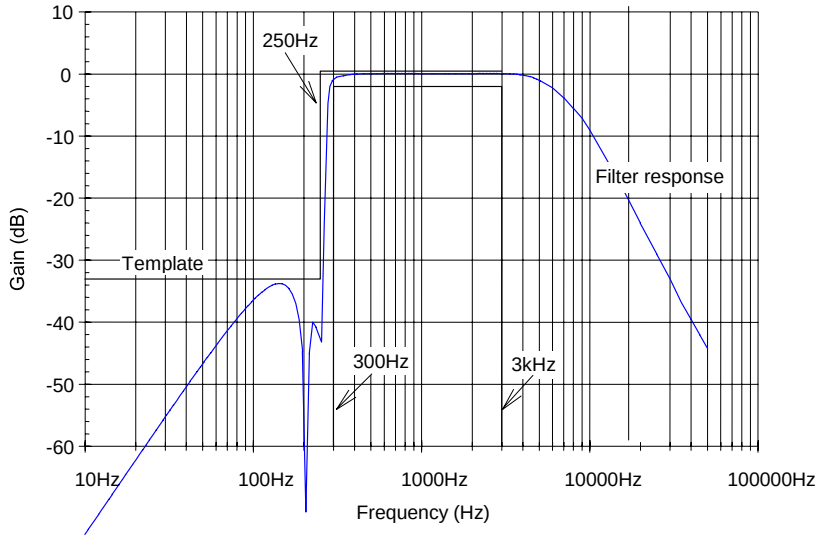


Figure 7 Rx Audio Filter Frequency Response

De-emphasis

Optional de-emphasis at -6dB per octave from 300Hz to 3000Hz (shown in Figure 8) can be selected, to facilitate compliance with TIA/EIA-603.

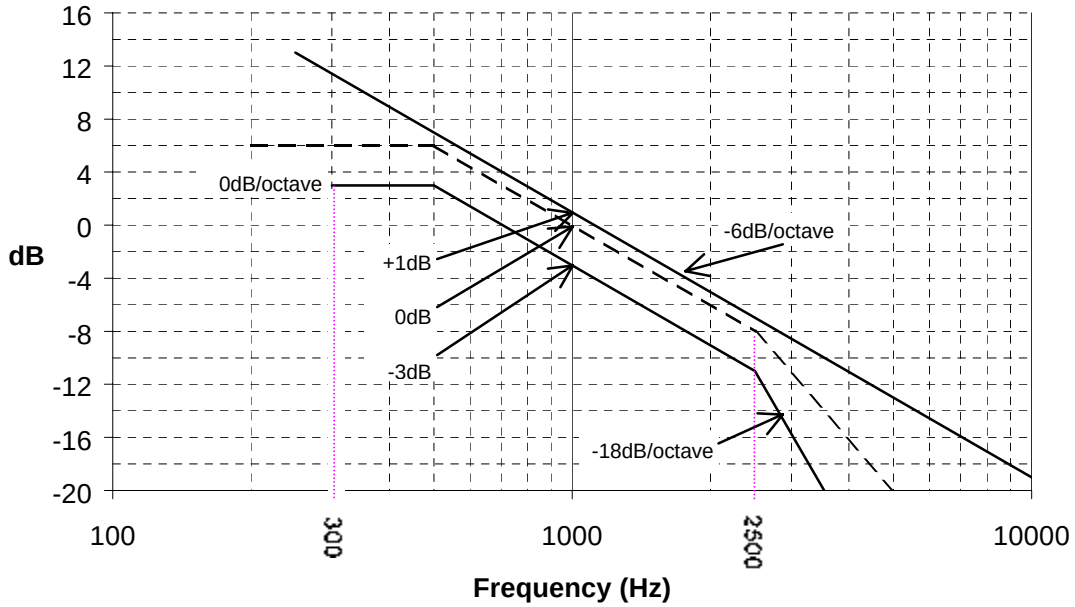


Figure 8 De-emphasis Curve for TIA/EIA-603 Compliance

Rx Companding (Expanding)

The CMX7041 incorporates an optional syllabic compandor in both transmit and receive modes. This expands received audio band signals that have been similarly compressed in the transmitter to enhance dynamic range. See section 6.5.3 and:

- Audio Control – $C2 write

Audio De-scrambling

The CMX7041 incorporates an optional frequency inversion de-scrambler in receive mode. This de-scrambles received audio band signals that have been scrambled in the transmitter.

See:

- Audio Control – $C2 write

6.5.2 Audio Transmit Mode

The device operates in half duplex, so when the device is in transmit mode the receive path (discriminator and audio output amplifiers) should be disabled, and can be powered down, by the host µC.

Two modulator outputs with independently programmable gains are provided to facilitate single or two-point modulation, separate sub-audio and audio band outputs. If one of the modulator outputs is not used it can be disabled to conserve power.

To avoid spurious transmissions when changing from Rx to Tx the MOD 1 and MOD 2 outputs are ramped to the quiescent modulator output level, V_{BIAS} before switching. Similarly, when starting a transmission, the transmitted signal is ramped up from the quiescent V_{BIAS} level and when ending a transmission the transmitted signal is ramped down to the quiescent V_{BIAS} level. The ramp rates are set in the Programming register P4.6. When the modulator outputs are disabled, their outputs will be set to V_{BIAS}. When the modulator output drivers are powered down, their outputs will be floating (high impedance), so the RF modulator will need to be turned off.

For all transmissions, the host µC must only enable signals after the appropriate data and settings for those signals are loaded into the C-BUS registers. As soon as any signalling is enabled the CMX7041 will use the settings to control the way information is transmitted.

A programmable gain stage in the microphone input path facilitates a host controlled VOGAD capability.

See:

- Audio Control – $C2 write

Processing Audio Signals for Transmission over Analogue Channels

The microphone input(s), with programmable gain, can be selected as the audio input source. Pre-emphasis is selectable with either of the two analogue Tx audio filters (for 12.5kHz and 25kHz channel spacing). These are designed for use in ETS-300-086 and/or TIA/EIA-603 compliant applications. Both filters attenuate sub-audio frequencies below 250Hz by more than 33dB with respect to the signal level at 1kHz when the 300Hz HPF is enabled. These filters, together with a built in limiter, help ensure compliance with ETS-300-086 (25kHz and 12.5kHz channel spacing) when levels and gain settings are set up correctly in the target system.

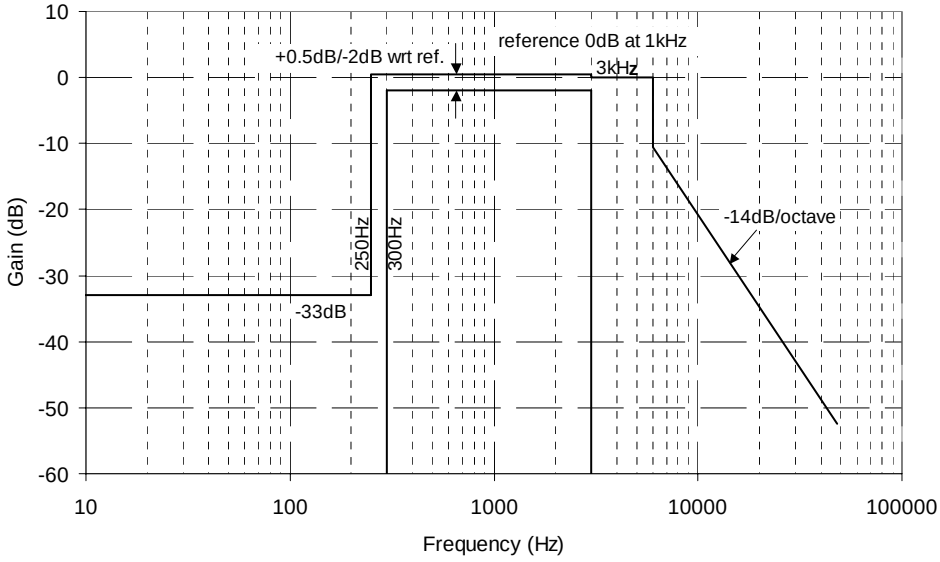


Figure 9 25kHz Channel Audio Filter Response Template

The filter characteristics of the 12.5kHz channel filter fit the filter template shown in Figure 10 (solid outline – with the 300Hz HPF active). This filter also facilitates implementation of systems compliant with TIA/EIA-603 'A' and 'B' bands. To achieve attenuation above 3kHz of better than –100dB/decade for TIA/EIA-603 'C' band (dashed outline), additional external circuitry is required.

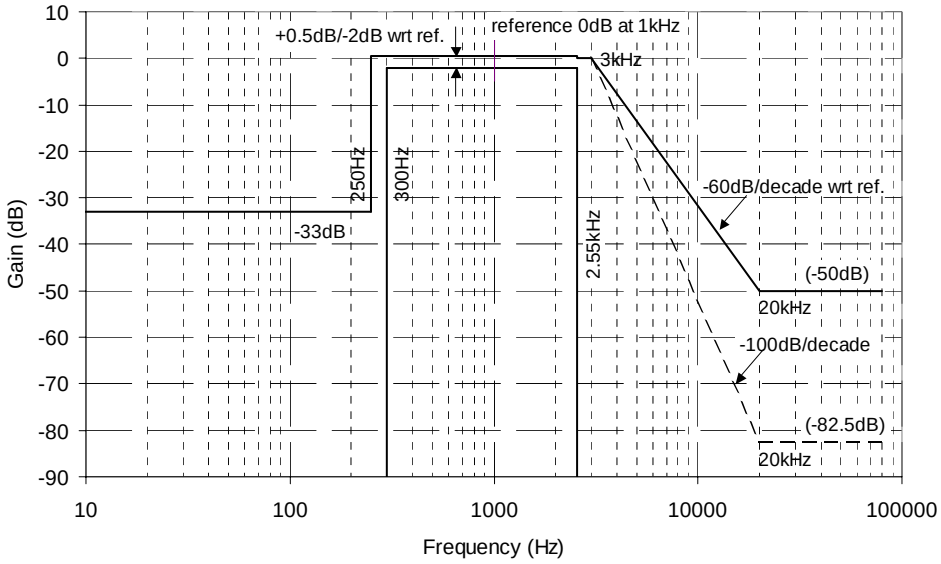


Figure 10 12.5kHz Channel Audio Filter Response Template

The CMX7041 provides selectable pre-emphasis filtering of +6dB per octave from 300Hz to 3000Hz, matching the template shown in Figure 11.

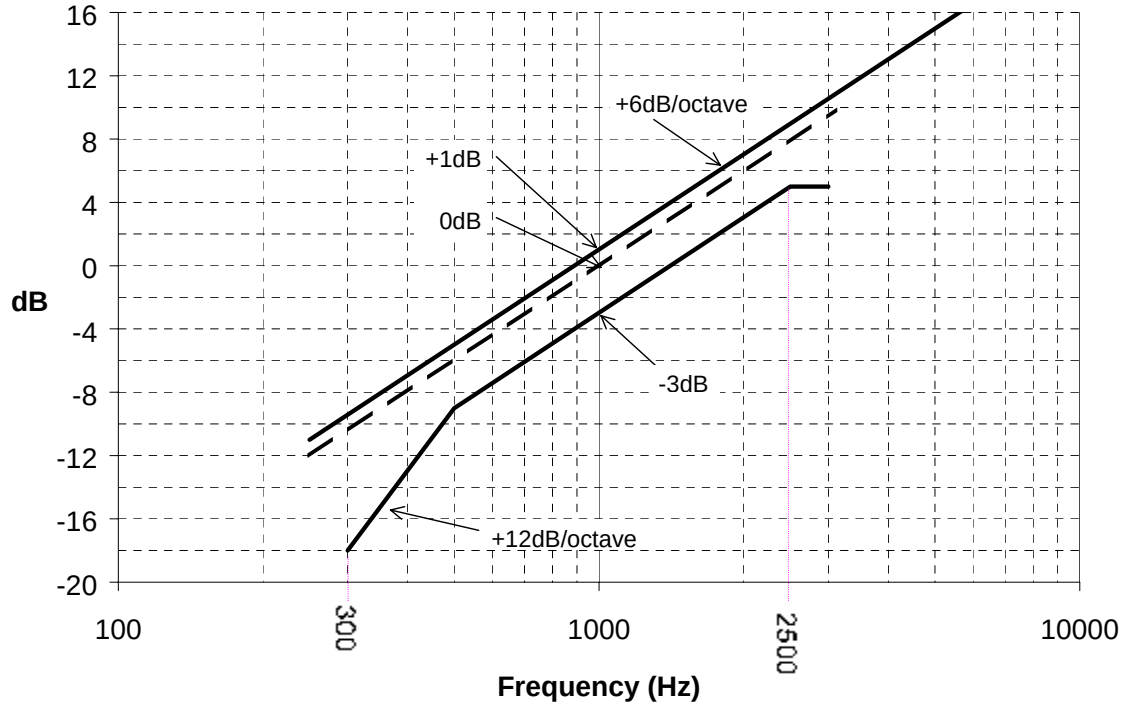


Figure 11 Audio Frequency Pre-emphasis Template

Modulator Output Routing

The sub-audio component can be combined with the audio band signal and this composite signal routed to both MOD1 and MOD2 outputs, or the sub-audio and audio band signal can be output separately (sub-audio to MOD2 and audio band to MOD1), in accordance with the settings of:

- o AuxADC and TX MOD mode - $A7 write
- o Input Gain and Output Signal Routing - $B1 write

Tx Companding (Compressing)
The CMX7041 incorporates an optional syllabic compandor in both transmit and receive mode. This compresses audio band signals before transmission to enhance dynamic range. See section 6.5.3 and:

- o Audio Control – $C2 write

Audio Scrambling
The CMX7041 incorporates an optional frequency inversion scrambler in transmit mode. This scrambles audio band signals, to be de-scrambled in the receiver.

See:
- o Audio Control – $C2 write

6.5.3 Audio Compandor

The compandor is comprised of a compressor and an expandor. The compressor's function is to reduce the dynamic range of a given signal by attenuating larger amplitudes while amplifying smaller amplitudes. The expandor's function is to expand the dynamic range of a given signal by attenuating small amplitude signals (e.g. noise) while amplifying large amplitude signals. The compressor is used prior to transmission and the expandor is used in the receiver. Hence, using a compandor will enhance performance in a communication system by transmitting a compressed signal, which is less likely to be corrupted by noise, and then at the receiver expanding the compressed signal, which will push the noise picked up during transmission down further.

The CMX7041 uses a "syllabic compandor." This type of compandor, as opposed to the instantaneous compandor (e.g. μ/A-law PCM), responds to changes in the average envelope of the signal amplitude according to a syllabic time constant τ. Typically the steady state output for the compressor is proportional to the square root of the input signal. Ie:, for a 2 dB change in input signal, the output change will be 1 dB. Generally for voice communication systems a compressor is expected to have an input dynamic range of 60 dB, providing an output dynamic range of 30 dB. The expandor does the inverse.

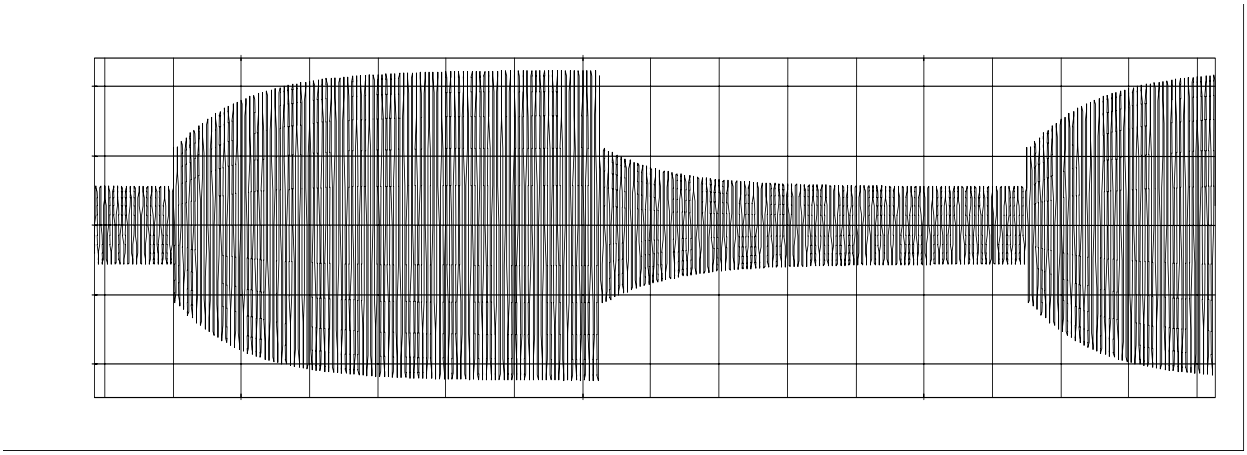


Figure 12 Expandor Transient Response

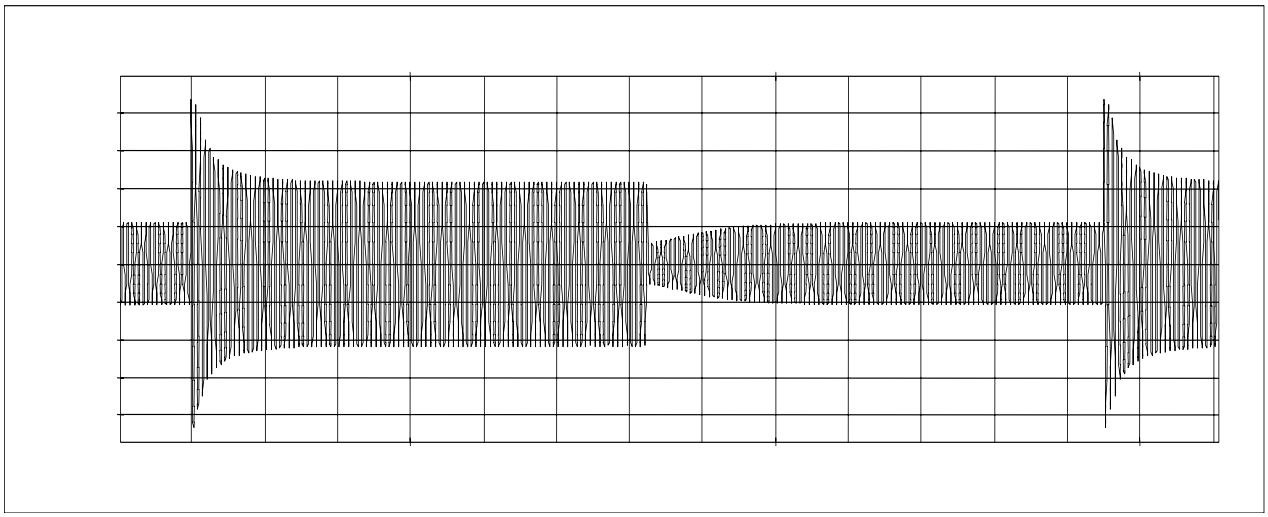


Figure 13 Compressor Transient Response

6.6 Sub-audio Signalling

Sub-audio signalling is available in the audio band below 260Hz. When sub-audio signalling is enabled, the 300Hz HPF in the audio section should also be enabled to remove the sub-audio signalling from the audio signal (in both Tx and Rx). Both CTCSS tones and DCS codes are supported, as well as a special "tone-cloning" mode which will report back any received CTCSS tone rather than look for a specific tone. There are 51 CTCSS tones defined in the CMX7041 and there is provision for a user-specified tone. Tone inversion to implement "Reverse Tone Burst" for squelch tail elimination can be accomplished by inverting the output of the MOD1 and MOD2 outputs ($B0).

The DCS coder / decoder supports both 23- and 24-bit modes with both true and inverse modulation formats and the 134Hz end of transmission burst.

The CTCSS tone and DCS code values for both Rx and Tx operation are specified in the Audio Control register ($C2), in the lowest 8 bits (shown in decimal):

- 0 no tone
- 1 to 83 DCS code 1 to 83
- 84 User-defined DCS code
- 101 to 183 Inverted DCS code 1 to 83
- 184 Inverted user-defined DCS code
- 200 CTCSS Tone Clone™ mode
- 201 to 254 CTCSS tones 1 to 51, User, XTCSS and DCSoff tones
- 255 Invalid tone

The CTCSS and DCS functions are enabled by the relevant bits in the Mode Control register, $C1, so that the host can turn the functionality on or off without having to re-program the values in the Audio Control register, $C2.

See:

- Analogue Output Gain - $B0 write
- Mode Control – $C1 write
- Audio Control – $C2 write

6.6.1 Receiving and Decoding CTCSS Tones

The CMX7041 is able to accurately detect valid CTCSS tones quickly to avoid losing the beginning of audio or data transmissions, and is able to continuously monitor the detected tone with minimal probability of falsely dropping out. The received signal is filtered in accordance with the template shown in Figure 14, to prevent signals outside the sub-audio range from interfering with the sub-audio tone detection.

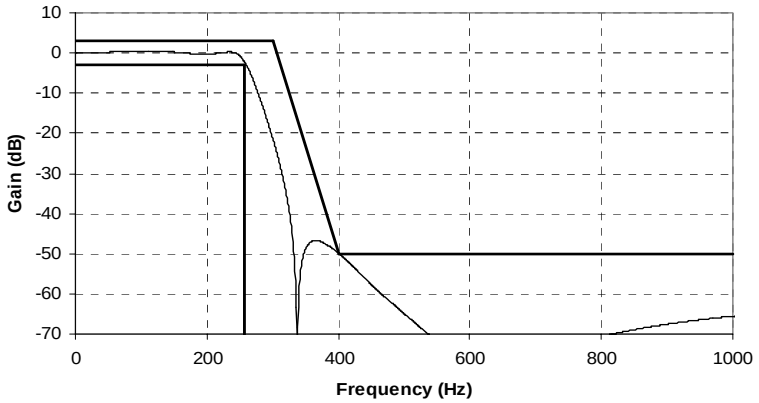


Figure 14 Low Pass Sub-Audio Band Filter for CTCSS and DCS

Once a valid CTCSS tone has been detected, Status register ($C6) b11 will be set and the host µC can then route the audio band signal to the audio output. The audio band signal is extracted from the received signal by band pass filtering as shown in Figure 7.

To optimise the CTCSS tone decoder, adjustable decoder bandwidths and threshold levels allow the user to trade-off decode certainty against signal to noise performance when congestion or range restrict the system performance. The tone decoder bandwidth and threshold level are set in P2.1 of the Programming register ($C8) and the desired tone is programmed in the Audio Control register ($C2). In systems which make use of tones 41 to 50 or other “split” tones (tones in between the frequencies of tones 1 to 40), the CTCSS decoder bandwidth should be reduced to avoid false detection of adjacent tones.

Tone Cloning™

Tone Cloning™ facilitates the detection of CTCSS tones 1 to 39 in receive mode which allows the device to non-predictively detect any tone in this range. This mode is activated by programming CTCSS Tone Number 00 (b0-7 of Audio Control = 200 decimal). The received tone number will be reported in the Tone Status register and can then be programmed into the Audio Control register by the host µC. The cloned tone will only be active when CTCSS is enabled in the Mode Control register. This setting has no effect in Tx mode and the CTCSS generator will output no signal.

Tone cloning™ should not be used in systems where tones 41 to 51 or other “split” tones (tones between the frequencies of tones 1 to 40) may be received. The all-call tone 40 can still be used after tone cloning has been performed. The CTCSS decoder detection bandwidth should be set to its lowest value (in P2.1 of the Programming Register) to ensure accurate detection.

CTCSS Tones

Table 3 lists the CTCSS tones available, the tone numbers and the equivalent (decimal) values that need to be programmed into the Audio Control register ($C2) and which will be reported back in the Tone Status register ($CC).

Table 3 CTCSS Tones

Register value (dec)	Tone Number	Frequency (Hz)	Register value (dec)	Tone Number	Frequency (Hz)	Register value (dec)	Tone Number	Frequency (Hz)
000	n/a	No Tone	218	18	123.0	237	37	241.8
200	0	ToneClone	219	19	127.3	238	38	250.3
201	1	67.0	220	20	131.8	239	39	69.3
202	2	71.9	221	21	136.5	240	40	*62.5*
203	3	74.4	222	22	141.3	241	41	*159.8*
204	4	77.0	223	23	146.2	242	42	*165.5*
205	5	79.7	224	24	151.4	243	43	*171.3*
206	6	82.5	225	25	156.7	244	44	*177.3*
207	7	85.4	226	26	162.2	245	45	*183.5*
208	8	88.5	227	27	167.9	246	46	*189.9*
209	9	91.5	228	28	173.8	247	47	*196.6*
210	10	94.8	229	29	179.9	248	48	*199.5*
211	11	97.4	230	30	186.2	249	49	*206.5*
212	12	100.0	231	31	192.8	250	50	*229.1*
213	13	103.5	232	32	203.5	251	51	*254.1*
214	14	107.2	233	33	210.7	252	52	User
215	15	110.9	234	34	218.1	253	53	XTCSS
216	16	114.8	235	35	225.7	254	54	DCSoff
217	17	118.8	236	36	233.6	255	55	Invalid

Tone Cloning™ is a trademark of CML Microsystems Plc.

Notes:

1. Register value 000 in b0-7 of the Tone Status register ($CC) indicates that none of the above sub-audio tones is being detected. If register value 000 is programmed into the Audio Control register ($C2) and CTCSS enabled in the Mode Control register ($C1), only CTCSS tone 40 (240 decimal) will be scanned for. If CTCSS transmit is selected, this tone setting will cause the CTCSS generator to output no signal.
2. Tone number 40 (240 decimal) provides an all-user CTCSS tone option; regardless of the subaudio tones set, the CMX7041 will report the presence of this tone whenever the CTCSS detector is enabled. This feature is useful for implementing emergency type calls e.g. all-call.
3. Tone number 55 (255 decimal) is reported in the Tone Status register ($CC), when CTCSS receive is enabled and a sub-audio tone is detected that does not correspond to the selected tone or the all-call tone (tone number 40). This could be a tone in the sub-audio band which is not in the table or a tone in the table which is not the selected tone or all-call tone.
4. Tones 40 to 51 (241 to 251 decimal) are not in the TIA-603 standard.
5. Tone number 52 (252 decimal) will select the User Programmable Tone value in Program Block 2 – CTCSS and DCS Setup:
6. Tone number 53 (253 decimal) will select the XTCSS call maintenance tone, 64.7Hz
7. Tone number 54 (254 decimal) will select the DCS turn-off tone, 134.4Hz.
8. Tone Clone, register value 200, is a write-only value to $C6. It will not be reported back in $CC.

6.6.2 Receiving and Decoding DCS Codes

DCS code is in NRZ format and transmitted at 134.4 ±0.4bps. The CMX7041 is able to decode any 23- or 24-bit pattern in either of the two DCS modulation modes defined by TIA/EIA-603 and described in Table 4. The CMX7041 can detect a valid DCS code quickly enough to avoid losing the beginning of audio transmissions.

Table 4 DCS Modulation Modes

Modulation Type:	Data Bit:	FM Frequency Change:
A	0	Negative frequency shift
	1	Positive frequency shift
B	0	Positive frequency shift
	1	Negative frequency shift

The CMX7041 detects the DCS code that matches the programmed code defined in the Audio Control register ($C2). Register values 1 to 83 will detect modulation type A (“true”) and register values 101 to 183 will detect modulation type B (“inverted”). A facility for a user-defined code is available via Program Block 2 – CTCSS and DCS Setup:

To detect the pre-programmed DCS code, the signal is low-pass filtered to suppress all but the sub-audio band, using the filter shown in Figure 14. Further equalisation filtering, signal slicing and level detection are performed to extract the code being received. The extracted code is then matched with the programmed 23- or 24-bit DCS code to be recognised, in the order least significant first through to most significant DCS code bit last. Table 5 shows a selection of valid 23-bit DCS codes: this does not preclude other codes being programmed. Recognition of a valid DCS code will be flagged if the decode is successful (3 or less errors) by setting b10 of the Status register ($C6) to 1. A failure to decode is indicated by clearing this bit to 0. This bit is updated after the decoding of every 4th bit of the incoming signal. The actual code received is reported back in the Tone Status register ($CC) according to Table 5, so that the host µC can determine if it was the true or inverted form of the code.

Once a valid DCS code has been detected, the host µC can route the audio band signal to the AUDIO output. The audio signal is extracted from the received input signal by band pass filtering, see Figure 7.

The end of DCS transmissions is indicated by a 134.4 ±0.5Hz tone for 150-200ms. When a valid DCS code has been detected, the CMX7041 will automatically scan for the turn-off tone. When a DCS turn off tone is detected it will cause a DCS interrupt and report tone 54 (Tone Status b0-7 value 254 decimal); the receiver audio output can then be muted by the host.

Table 5 DCS 23 Bit Codes

Reg value True	Reg value Invert	**DCS Code**	DCS bits 22-12	DCS bits 11-0	Reg value True	Reg value Invert	**DCS Code**	DCS bits 22-12	DCS bits 11-0	Reg value True	Reg value Invert	**DCS Code**	DCS bits 22-12	DCS bits 11-0
1	*101*	**023**	763	813	*29*	*129*	**174**	18B	87C	*57*	*157*	**445**	7B8	925
2	*102*	**025**	6B7	815	*30*	*130*	**205**	6E9	885	*58*	*158*	**464**	27E	934
3	*103*	**026**	65D	816	*31*	*131*	**223**	68E	893	*59*	*159*	**465**	60B	935
4	*104*	**031**	51F	819	*32*	*132*	**226**	7B0	896	*60*	*160*	**466**	6E1	936
5	*105*	**032**	5F5	81A	*33*	*133*	**243**	45B	8A3	*61*	*161*	**503**	3C6	943
6	*106*	**043**	5B6	823	*34*	*134*	**244**	1FA	8A4	*62*	*162*	**506**	2F8	946
7	*107*	**047**	0FD	827	*35*	*135*	**245**	58F	8A5	*63*	*163*	**516**	41B	94E
8	*108*	**051**	7CA	829	*36*	*136*	**251**	627	8A9	*64*	*164*	**532**	0E3	95A
9	*109*	**054**	6F4	82C	*37*	*137*	**261**	177	8B1	*65*	*165*	**546**	19E	966
10	*110*	**065**	5D1	835	*38*	*138*	**263**	5E8	8B3	*66*	*166*	**565**	0C7	975
11	*111*	**071**	679	839	*39*	*139*	**265**	43C	8B5	*67*	*167*	**606**	5D9	986
12	*112*	**072**	693	83A	*40*	*140*	**271**	794	8B9	*68*	*168*	**612**	671	98A
13	*113*	**073**	2E6	83B	*41*	*141*	**306**	0CF	8C6	*69*	*169*	**624**	0F5	994
14	*114*	**074**	747	83C	*42*	*142*	**311**	38D	8C9	*70*	*170*	**627**	01F	997
15	*115*	**114**	35E	84C	*43*	*143*	**315**	6C6	8CD	*71*	*171*	**631**	728	999
16	*116*	**115**	72B	84D	*44*	*144*	**331**	23E	8D9	*72*	*172*	**632**	7C2	99A
17	*117*	**116**	7C1	84E	*45*	*145*	**343**	297	8E3	*73*	*173*	**654**	4C3	9AC
18	*118*	**125**	07B	855	*46*	*146*	**346**	3A9	8E6	*74*	*174*	**662**	247	9B2
19	*119*	**131**	3D3	859	*47*	*147*	**351**	0EB	8E9	*75*	*175*	**664**	393	9B4
20	*120*	**132**	339	85A	*48*	*148*	**364**	685	8F4	*76*	*176*	**703**	22B	9C3
21	*121*	**134**	2ED	85C	*49*	*149*	**365**	2F0	8F5	*77*	*177*	**712**	0BD	9CA
22	*122*	**143**	37A	863	*50*	*150*	**371**	158	8F9	*78*	*178*	**723**	398	9D3
23	*123*	**152**	1EC	86A	*51*	*151*	**411**	776	909	*79*	*179*	**731**	1E4	9D9
24	*124*	**155**	44D	86D	*52*	*152*	**412**	79C	90A	*80*	*180*	**732**	10E	9DA
25	*125*	**156**	4A7	86E	*53*	*153*	**413**	3E9	90B	*81*	*181*	**734**	0DA	9DC
26	*126*	**162**	6BC	872	*54*	*154*	**423**	4B9	913	*82*	*182*	**743**	14D	9E3
27	*127*	**165**	31D	875	*55*	*155*	**431**	6C5	919	*83*	*183*	**754**	20F	9EC
28	*128*	**172**	05F	87A	*56*	*156*	**432**	62F	91A	*84*	*184*	User Defined		

Notes:

1. Register value 84 will select the User Programmable DCS code value in Program Block 2 – CTCSS and DCS Setup: Register value 184 will select the Inverted form of the User Programmable DCS code.
2. Note that the Audio Control register values are shown in decimal.

6.6.3 Transmit CTCSS Tone

The sub-audio CTCSS tone generated is defined in the Audio Control register ($C2). Table 3 lists the CTCSS tones and the corresponding decimal values for programming b0-7 of the register.

6.6.4 Transmit DCS Code

A 23- or 24-bit sub-audio DCS code can be generated, as defined by the Audio Control register ($C2). The same DCS code pattern is used for detection and transmission. The DCS code is NRZ encoded at 134.4±0.4 bps, low-pass filtered and added to the audio band signal, before being passed to the modulator output stages. Valid 23-bit DCS codes and the corresponding settings for the Audio Control Register are shown in Table 5, and include a user-defined facility. The least significant bit of the DCS code is transmitted first and the most significant bit is transmitted last. The CMX7041 is able to encode and transmit either of the two DCS modulation modes defined by TIA/EIA-603 (true and inverted) described in Table 4. If 24-bit mode is required, bit 11 of Programming register P2.1 should be set.

To signal the end of the DCS transmission, the host should set the Audio Control register ($C2) to the DCS turn off tone (register value b0-7 = 254 decimal) for 150ms to 200ms. After this time period has elapsed the host should then disable DCS in the Mode Control register ($C1).

6.7 Inband Signalling – Selcall / DTMF / User Tones

The CM7041 supports both Selcall, DTMF (Tx only) and user-programmable In-band tones between 288Hz and 3000Hz. Note that if tones below 400Hz are used, sub-audio signalling should be disabled and the 300Hz HPF disabled.

By default, the CMX7041 will load the EEA Selcall tone set, however this may be over-written by the host with any valid set of tones within its operational range by use of the Programming register. This ensures that the device can remain compatible with all available tone systems in use. The CMX7041 does not implement automatic repeat tone insertion or deletion: it is up to the host to correctly implement the appropriate Selcall protocol.

Selection of the In-band signalling mode is performed by bits 11-9 of the Mode register ($C1). Detection of the selected In-band signalling mode can be performed in parallel with audio or data reception.

See:
- Mode Control – $C1 write
- Tx In-band Tones - $C3 write
- Tone Status - $CC read

6.7.1 Receiving and Decoding In-band Tones

In-band tones can be used to flag the start of a call or to confirm the end of a call. If they occur during a call the tone may be audible at the receiver. When enabled, an interrupt will be issued when a signal matching a valid In-band tone changes state (ie: on, off or a change to different tone).

The CMX7041 implements QTC coding using the EEA tone set. Other addressing and data formats can be implemented, but will require more host intervention. The custom tones (1-4) permit other audio tones to be encoded or decoded. The frequency of each tone is defined in the Programming registers P1.10 to P1.13.

In receive mode the CMX7041 scans through the tone table sequentially. The code reported will be the first one that matches the incoming frequency.

Adjustable decoder bandwidths and threshold levels are programmable via the Programming register. These allow certainty of detection to be traded against signal to noise performance when congestion or range limits the system performance. The In-band signal is derived from the received input signal after the band pass filtering shown in Figure 7.

Table 6 In-band Tones

Custom Tones: (b15 = 0)			Selcall Tones: (b15 = 1)		
b14 - 11		Freq.	b14 - 11		Freq.
Dec	Hex	(Hz)	Dec	Hex	(Hz)
0	0	No Tone	0	0	1981
1	1	Custom Tone 1 P1.10[1]	1	1	1124
2	2	Custom Tone 2 P1.11[1]	2	2	1197
3	3	Custom Tone 3 P1.12[1]	3	3	1275
4	4	Custom Tone 4 P1.13[1]	4	4	1358
5	5	Reserved	5	5	1446
6	6		6	6	1540
7	7		7	7	1640
8	8		8	8	1747
9	9		9	9	1860
10	A		10	A	1055
11	B		11	B	930
12	C		12	C	2247
13	D		13	D	991
14	E		14	E	2110[2]
15	F	Unrecognised Tone	15	F	Unrecognised Tone

Notes:

1 Special tones 1-4 provide user programmable tone options for both transmit and receive modes as set in the indicated Program register, for programming information see section 8.2.2 in the CMX7041 User Manual.

2 Normally, tone 14 is the repeat tone. This code must be used in transmit mode when the new code to be sent is the same as the previous one. e.g. to send '333' the sequence '3R3' should be sent, where 'R' is the repeat tone. When receiving Selcall tones, the CMX7041 will indicate the repeat tone when it is received. It is up to the host to interpret and decode the tones accordingly.

6.7.2 Transmitting In-band Tones

The In-band tone to be generated is defined in the TX TONE register ($C3). The tone level is set in the Programming register (P1.4). The In-band tone must be transmitted without other signals in the audio band, so the host µC must disable the audio or data paths prior to initiating transmission of an In-band tone and restore them after the In-band tone transmission is complete. Table 6 shows valid In-band tones, together with the values for programming the In-band bits of the TX Inband Tones register.

Custom In-band tone frequencies are set in P1.10-13 of the Programming register ($C8). See section 8.2.2 in the CMX7041 User Manual for programming details.

6.7.3 Transmitting DTMF Tones

The DTMF signals to be generated are defined in the TX TONE register ($C3). Single tones and twist (lower frequency tone reduced by 2dB) can be enabled by setting the appropriate bit in the $C3 register to '1'. The DTMF level is set in programming register P1.0. The DTMF tones must be transmitted on their own, the host µC must disable audio band signals prior to initiating transmission of the DTMF tones and (if required) restore the audio band signals after the DTMF transmission is complete. Table 7 shows the DTMF tone pairs, together with the values for programming the 'Tone Pair' field of the TX TONE register.

Table 7 DTMF Tone Pairs

Tone Pair Programming Code (Hex)	Key Pad Position	Low Tone (Hz)	High Tone (Hz)
1	1	697	1209
2	2	697	1336
3	3	697	1477
4	4	770	1209
5	5	770	1336
6	6	770	1477
7	7	852	1209
8	8	852	1336
9	9	852	1477
A	0	941	1336
B	*	941	1209
C	#	941	1477
D	A	697	1633
E	B	770	1633
F	C	852	1633
0	D	941	1633

Note: Only the underlined tone is generated when the 'Single Tone' bit is enabled.

6.7.4 Alternative Selcall Tone Sets

These may be loaded via the Programming register to locations P1.6 to P1.21. See section 8.2.2 in the CMX7041 User Manual.

Table 8 Alternative Selcall Tone Sets

	EIA	EEA	CCIR	ZVEI 1	ZVEI 2
Tone Number	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)
0	600	1981	1981	2400	2400
1	741	1124	1124	1060	1060
2	882	1197	1197	1160	1160
3	1023	1275	1275	1270	1270
4	1164	1358	1358	1400	1400
5	1305	1446	1446	1530	1530
6	1446	1540	1540	1670	1670
7	1587	1640	1640	1830	1830
8	1728	1747	1747	2000	2000
9	1869	1860	1860	2200	2200
A (10)	2151	1055	2400	2800	885
B (11)	2435	930	930	810	810
C (12)	2010	2247	2247	970	740
D (13)	2295	991	991	885	680
E (14)	459	2110	2110	2600	970
F (15)	NoTone	2400	1055	680	2600

6.8 Data Functions

The CMX7041 supports both 1200 and 2400 bps MSK / FFSK data modes. In Rx mode, the device can be set to look for either mode, however, once a valid mode has been found, it will stay in that mode until the host resets it.

See:

- Mode Control – $C1 write
- Modem Control - $C7 write
- Rx Data 1 - $C5 read and Rx Data 2 and XTCSS - $C9 read
- XTCSS and Tx Data 1 and 2 - $CA and CB write

6.8.1 Receiving FFSK / MSK Signals

The CMX7041 can decode incoming FFSK/MSK signals at either 1200 or 2400 baud data rates, automatically detecting the rate from the received signal. Alternatively, a control word may set the baud rate, in which case the device only responds to signals operating at that rate. The form of FFSK/MSK signals for these baud rates is shown in Figure 15.

The received signal is filtered and data is extracted with the aid of a PLL to recover the clock from the serial data stream. The recovered data is stored in a 2- or 4-byte buffer (grouped into 16-bit words) and an interrupt issued to indicate received data is ready. Data is transferred over the C-BUS under host µC control. If this data is not read before the next data is decoded it will be overwritten and it is up to the user to ensure that the data is transferred at an adequate rate following data ready being flagged, see Table 11. Typical Bit and Block Error Rate performance is shown in Figure 18 and Figure 19. The MSK bit clock is not output externally.

The extracted data is compared with the 16-bit programmed Frame Sync pattern (preset to $CB23 following a RESET command). An interrupt will be flagged when the programmed Frame Sync pattern is detected or when the following Frame Head is decoded, see section 6.9.3. The host µC may stop the frame sync search by disabling the MSK demodulator.

If the CMX7041 has been set to decode a Frame Head before interrupting, it will check the CRC portion of the Frame Head Control Field. If this indicates a corrupt Frame Head then a search for a new frame sync pattern will be automatically restarted.

FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component. The device will handle the sub-audio signals as previously described. If a sub-audio signal turns off during reception of FFSK, it is up to the host µC to turn off the FFSK decoding as the device will continue receiving and processing the incoming signal until commanded otherwise by the host µC.

The host µC must keep track of the message length or otherwise determine the end of reception (e.g. by using sub-audio information to check for signal presence) and disable the FFSK demodulator at the appropriate time. Note that when using packets with embedded size information, the CMX7041 will indicate when the last data block has been received.

6.8.2 Transmitting FFSK/MSK Signals

The FFSK/MSK encoding operates in accordance with the bit settings in the Modem Control register ($C7). When enabled the MSK modulator will begin transmitting data using the settings and values in block 0 of the Programming register (bit sync and frame sync patterns), the Modem Control register and the TX Data registers. Therefore, these registers should be programmed to the required values before transmission is enabled.

The CMX7041 generates its own internal data clock and converts the binary data into the appropriately phased frequencies, as shown in Figure 15 and Table 9. The binary data is taken from TX DATA #1 and #2 registers ($CA and $CB), most significant bit first. The following data words must be provided over the C-BUS within certain time limits to ensure the selected baud rate is maintained. The time limits will be dependent on the data coding being used, see Table 11.

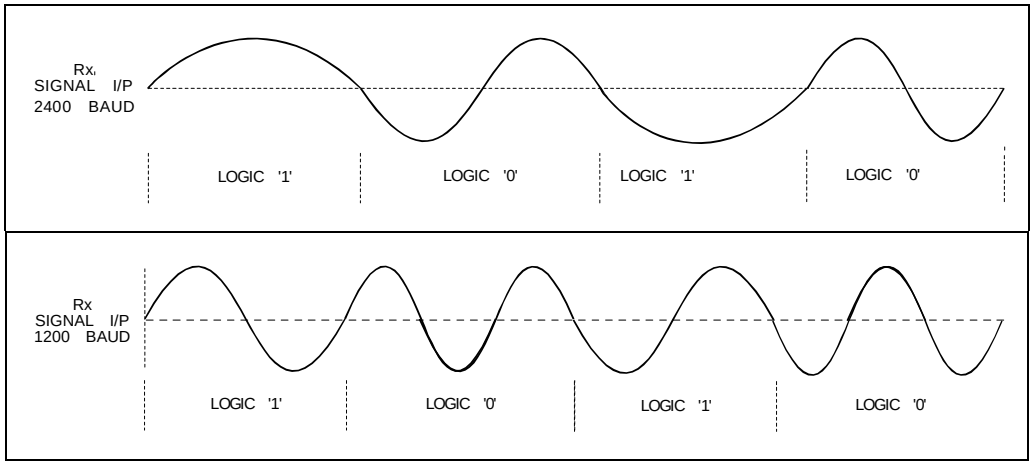


Figure 15 Modulating Waveforms for 1200 and 2400 Baud FFSK/MSK Signals

The table below shows the combinations of frequencies and number of cycles to represent each bit of data, for both baud rates.

Table 9 Data Frequencies for each Baud Rate

Baud Rate	Data	Frequency	Number of Cycles
1200baud	1	1200Hz	one
	0	1800Hz	one and a half
2400baud	1	1200Hz	half
	0	2400Hz	one

Note: FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component.

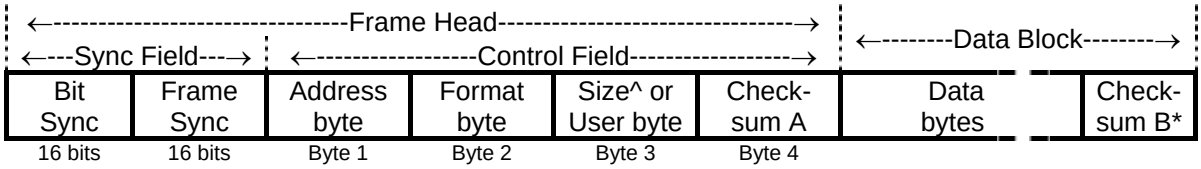
6.9 FFSK/MSK Data Packetizing

The CMX7041 has extensive data packetizing features that can be controlled by the Modem Control register ($C7). The CMX7041 can packetize data in a variety of formats so the user can have the optimum data throughput for various signal to noise ratios. Data is transferred in packets or frames, each frame is made up of a Frame Head followed by any associated User Data. The Frame Head is composed of a 16-bit Bit Sync and 16-bit Frame Sync pattern immediately followed by 4 bytes of data. The 4 bytes of data start with an 8-bit address followed by 1 byte carrying information about the format of the following data block, a further byte indicates the size of the packet and the last byte is a checksum to detect if any of the 4 Frame Head bytes has been corrupted.

6.9.1 Tx Hang Bit

When transmitting FFSK/MSK data of types 0, 2 or 3, the user should ensure that the data is terminated with a hang bit. To do this, the host must set the 'Last Data' bit in the Modem Control register ($C7) after the last data word has been loaded into the Tx Data #1 register ($CA), as described in section 8.1.25 in the CMX7041 User Manual. This will append a hang bit onto the end of the current word and will stop modulating after the hang bit has been transmitted. It will also generate an interrupt (if enabled) when the hang bit has left the modulator.

6.9.2 Frame Format



* Checksum B not applied to all Data Block types
^ Byte 3 is only reserved on sized data blocks.

The Data Block is made up from the User Data. This consists of a variable number of data bytes optionally encoded to ensure secure delivery over a radio channel to the receiver. Checksum B is only applied at the end of sized Data Blocks, the receiver can then detect if any of the User Data has been corrupted. Checksum B is composed of 16 bits for messages ≤16 bytes and 32 bits for longer messages.

6.9.3 Frame Head

The Frame Head forms an important part of a frame as it allows the receiver to detect and lock on to FFSK/MSK signals, provides basic addressing to screen out unwanted messages and indicates the format, coding and length of any following data.

The four Control Field bytes have Forward Error Correction (FEC) applied to them in the transmitter, this adds 4 bits to every byte and the receiver can correct errors in the received bytes. The 4 received bytes are then checked for a correct CRC, so that corrupted Frame Heads can be rejected. If checksum A indicates that the Control Field bytes are correct, the Address (byte 1) is compared with that stored in the MSK Header Address bits of Modem Address register, $B6 (b15:8). If a match occurs, or if the received address is '40', then an interrupt is raised indicating a valid Frame Head has been received. The Frame Head is 80 bits long (16 + 16 + {4x12}). The contents of a received Frame Head can be read from Rx Data registers $C5 and $C9.

6.9.4 Data Block Coding

The Data Block follows the Frame Head and can be coded with different levels of error correction and detection. The Data Block format is controlled by Frame Head byte 2, see also section 8.1.22 in the CMX7041 User Manual. Messages can take the following formats:

Type: Description:

0 **Raw Data**. The CMX7041 will transmit 16 bits at a time. In receive, the device will search for the programmed 16-bit Frame Sync pattern and then output all following data 16 bits at a time. The host will have to perform all other data formatting. The data scrambler does not operate in this mode. This mode can be useful when interfacing to a system using a different format to those available in the CMX7041.

1 **Frame Head only**. No User Data will be added. This format can be useful for indicating channel or user status by using byte 3 and the User Bit of the Frame Head (see section 8.1.22 in the CMX7041 User Manual).

2 **Frame Head followed by raw data**. User data is appended to the Frame Head in 2-byte units with no formatting or CRC added by the CMX7041. No size information is set in the Frame Head and User Data may contain any even number of bytes per Frame.

3 **Frame Head followed by FEC coded data only**. Each byte of the User Data has 4 bits of FEC coding added. No size information is set in the Frame Head and User Data may contain any even number of bytes per Frame. No CRC is added to the data.

4 **Frame Head followed by FEC coded data with an automatic CRC** at the end of the User Data. The number of User Data bytes in the Frame must be set in Frame Head byte 3. The CRC is automatically checked in the receiver and the result indicated to the host µC. Up to 255 bytes of User Data can be sent in each Frame using this format.

5 **As '4 above', with the addition of all Data Block bytes being interleaved**. This spreads the transmitted information over time and helps reduce the effect of errors caused by fading. Interleaving is performed on blocks of 4 bytes, the CMX7041 automatically adds and strips out pad bytes to ensure multiples of 4 bytes are sent over the radio channel.

Notes:

- Message types 1, 2 and 3 have no size information requirement and do not reserve Frame Head byte 3. This byte may be freely used by the host µC to convey information. In message types 4 and 5 this byte must be set to the number of User Bytes in the message attached to that Frame Head (≤255) to allow the receiver to correctly decode and calculate the CRC.
- Type 0 data transfers do not use frame heads. In Tx the host µC must transfer the bit and frame sync data before sending the message data. In Rx the host µC must decode all data after the frame sync.
- When using type 0 (raw data) messages it is strongly recommended that the default Frame Sync pattern is not used. This is to reduce the loading on receivers using the formatted data types, which would otherwise try to decode the 6 bytes following a type 0 Frame Sync as a Frame Head.

Table 10 Data Block Formatting Types

Data Block Formatting Type:	Total over-air bits for an 80-byte message	Air time for FFSK message (ms) at 1200baud	Air time for FFSK message (ms) at 2400baud	Over air efficiency	Burst length protection at 1200baud *[for 2400baud divide both times by 2]*	Probability of detecting errors
2	720	600	300	89%	None	Zero
3	1040	867	433	62%	<0.83ms in any 10ms	Poor
4	1088	907	453	59%	<0.83ms in any 10ms	Excellent
5	1088	907	453	59%	<3.33ms in any 40ms	Excellent

Higher levels of error protection have the penalty of adding extra bits to the over air signal and this reduces the effective bit rate. Less error protection increases the effective bit rate, however in typical radio conditions the penalty is a greater risk of errors leading to repeated messages and a net reduction in effective bit rate compared to using error correction and detection.

6.9.5 Data Scrambling/Privacy Coding

It is preferable for FFSK/MSK over-air data to be reasonably random in nature to ensure the receiver can track timing using the bit changes and to smooth the frequency spectrum. To reduce the possibility of user data causing long strings of 1's or 0's to be transmitted, a 16-bit data scrambler is provided and operates on all bits after the Frame Head.

The default (standard) setting for this scrambler is with a start code (seed) of $FFFF and any receivers with the same seed may decode this data. However, if the transmitter and receiver pre-arrange a different seed then the scrambler will start its sequence in another place and any simple receiver that does not know the transmitted seed will not be able to successfully decode the data. This method gives over 65,000 different starting points and the chance of others decoding data successfully is reduced.

The CMX7041 provides the option of two custom 16-bit words that are programmable by the user in Programming register P0.8 to P0.9. Bits 0 and 1 in the Frame Head Format byte indicate which setting (standard, Seed1, Seed2 or none) the following Data Block has been scrambled with, see section 8.2.1 in the CMX7041 User Manual. Note that a seed of $0000 will effectively turn off the scrambler and provide no protection against long sequences of 1's or 0's. Reception of scrambled data will only be successful when the receiving device has been programmed with the correct (identical) seed to that used by the transmitter.

By using this method the CMX7041 provides a privacy code that will protect against casual monitoring, however the data is not encrypted and a sophisticated receiver can decode the data by using moderately simple decoding techniques. If data encryption is required it must be performed by the host µC. The scrambler function is controlled by bits 0,1 of the Modem Control register, $C7.

6.9.6 Data Buffer Timing

Data must be transferred at the rate appropriate to the signal type and data format. The CMX7041 buffers data in two 16-bit registers. The CMX7041 will issue interrupts to indicate when data is available or required. The host must respond to these interrupts within the maximum allowable latency for the signal type. Table 11 shows the maximum latencies for transferring signal data to maintain appropriate data throughput.

Table 11 Maximum Data Transfer Latency

Data encoding type	Max. time to read from or write to data buffer		Data buffer size
	1200 baud	2400 baud	
0	13.3ms	6.6ms	2 bytes
1	N/A*	N/A*	4 bytes
2	13.3ms	6.6ms	2 bytes
3	20ms	10ms	2 bytes
4	40ms	20ms	4 bytes
5	40ms	20ms	4 bytes

* Type 1 message is an isolated Frame Head, there is no subsequent data to load (Tx) or read (Rx).

6.10 Auxiliary ADC Operation

The inputs to the two Auxiliary ADCs can be independently routed to any of the Signal Input pins under control of the Signal Routing register, $A7. Conversions will be performed as long as a valid input source is selected, to stop the ADCs, the input source should be set to “none”. Register $C0, b6, BIAS, must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the Signal Routing register, $A7, the length of the averaging is determined by the value in the Programming register (P3.0 and P3.1), and defaults to a value of 1. This is a rolling average system such that a proportion of the current data will be added to the last value. The proportion is determined by the value of the average counter in P3.0 and P3.1. For an average value of 0; 50% of the current value will be applied, for a value of 1 = 25%, 2 = 12.5% etc. The maximum useful value of this field is 8.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated as required (except in the case where the high threshold has been set below the low threshold). The thresholds are programmed via the AuxADC Threshold register, $B5.

Auxiliary ADC data is read back in the AuxADC Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:

- AuxADC and TX MOD mode - $A7 write
- AuxADC1 data - $A9 read
- AuxADC2 data - $AA read
- AuxADC threshold data - $B5 write

6.11 Auxiliary DAC / RAMDAC Operation

The four Auxiliary DAC channels are programmed via the AuxDAC Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Control register, $A8, with b12 set, controls this mode of operation. The default profile is a raised cosine (see Table 14), but this may be over-written with a user defined profile by writing to Programming register P3.10. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to IDLE or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

See:

- AuxDAC control / data - $A8 write

6.12 Digital System Clock Generators

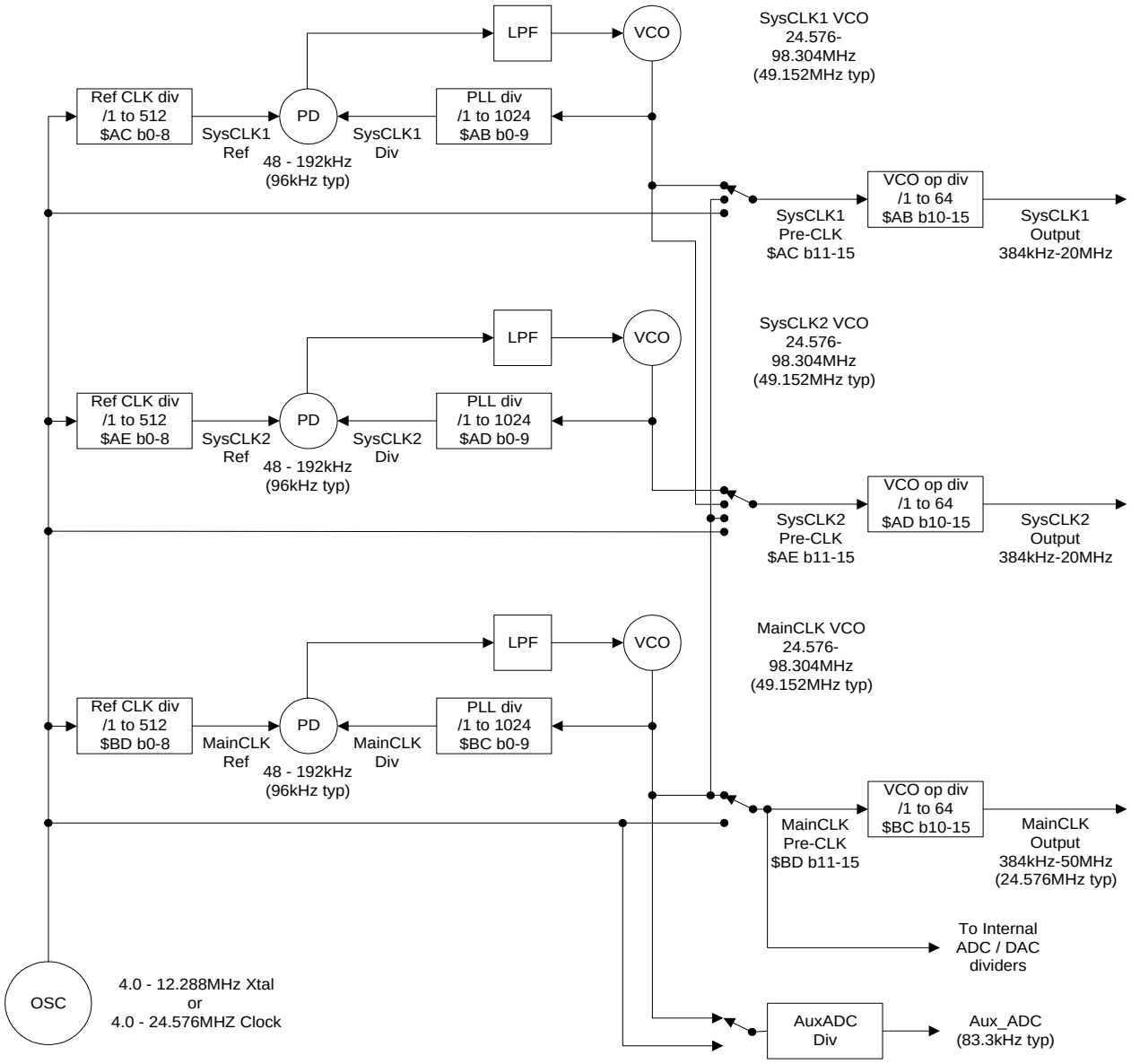


Figure 16 Digital Clock Generation Schemes

The CMX7041 includes a 2-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section 4, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 6.144MHz Xtal is assumed for the functionality provided in the CMX7041.

6.12.1 System Clock Operation

Two System Clock outputs, SysClock1 Out and SysClock2 Out, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 16. Note that at power-on, these pins provide, by default, a clock which is equivalent to the XTAL frequency.

See:

- o System CLK 1 and 2 PLL data - $AB, $AD write
- o System CLK 1 and 2 REF - $AC and $AE write

6.12.2 Main Clock Operation

A digital PLL is used to create the Main Clock (nominally 24.576MHz) for the internal sections of the CMX7041. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose Timer and the signal processing block. In particular, it should be noted that in IDLE mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX7041 defaults to the settings appropriate for a 6.144MHz Xtal, however if other frequencies are to be used then the Program Block registers P3.2 to P3.6 will need to be programmed appropriately at power-on. A table of common values is provided in Table 1. The C-BUS registers $BC and $BD are controlled automatically by the FI and must not be accessed by the user.

See:

- o Program Block 3 – AuxDAC, RAMDAC and Clock control:

6.13 GPIO

Two pins are provided for GPIO purposes. Their function is determined by the Function Image™ code and these pins are not accessible to the user via C-BUS. With the current version of the FI, these pins are reserved for future use and should be left unconnected.

6.14 Signal Level Optimisation

The internal signal processing of the CMX7041 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3V)] Volts pk-pk = 838mV rms, assuming a sine wave signal. Compared to the reference level of 308mV rms, this is a signal of +8.69dB. This should not be exceeded at any stage.

6.14.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Analogue Routing block should not exceed +8.69dB, assuming both fine and coarse output attenuators are set to a gain of 0dB. The sub-audio level is normally set to 31mV rms ±1.0dB, which means that the output from the soft limiter must not exceed 803mV rms. If pre-emphasis is used, an output signal at 3000Hz will have three times the amplitude of a signal at 1000Hz, so the signal level before pre-emphasis should not exceed 268mV rms. If the compressor is also used, its 'knee' is at 100mV rms, which would allow a signal into the compressor of 718mV rms, which is less than the maximum signal level. The Fine Input Gain adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input Gain adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the MicFB pin would be 54mV rms. With the lowest gain setting (0dB), the maximum allowable input signal level at the MicFB pin would be 718mV rms.

6.14.2 Receive Path Levels

For the maximum signal out of the AUDIO attenuator, the signal level at the output of the Analogue Routing block should not exceed +8.69dB, assuming both fine and coarse output attenuators are set to a gain of 0dB. In this case, there is no sub-audio signal to be added, so the maximum signal level remains at 838mV rms. If de-emphasis is used, an output signal at 300Hz will have three and a third times the amplitude of a signal at 1000Hz, so the signal level before de-emphasis should not exceed 251mV rms. If the expander is also used, its 'knee' is at 100mV rms, which would allow a signal into the expander of 158mV rms. The Fine Input Gain adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input Gain adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the DiscFB pin would be 12.0mV rms. With the lowest gain setting (0dB), the maximum allowable input signal level at the DiscFB pin would be 158mV rms. The signal level of +8.69dB (838mV rms) is an absolute maximum, which should not be exceeded anywhere in the signal processing chain if severe distortion is to be avoided.

6.15 C-BUS Register Summary

Table 12 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC and TX MOD Mode	16
$A8	W	AuxDAC Data and Enable	16
$A9	R	AuxADC1 Data and Status / Checksum 2 hi	16
$AA	R	AuxADC2 Data and Status / Checksum 2 lo	16
$AB	W	System Clk 1 PLL configure	16
$AC	W	System Clk 1 Ref configure	16
$AD	W	System Clk 2 PLL configure	16
$AE	W	System Clk 2 Ref configure	16
$AF		Reserved	
$B0	W	Analog Output Gain	16
$B1	W	Input Gain and Signal Routing	16
$B2		Reserved	
$B3		Reserved	
$B4		Reserved	
$B5	W	AuxADC Thresholds	16
$B6	W	Modem Address	16
$B8	R	Checksum 1 hi	16
$B9	R	Checksum 1 lo	16
$BB	R	NWR Status and Data	16
$BC	W	Main CLK PLL configure	16
$BD	W	Main CLK Ref configure	16
$BE		Reserved	
$BF		Reserved	
$C0	W	Power-Down Control	16
$C1	W	Mode Control	16
$C2	W	Audio Control	16
$C3	W	Tx In-band Tones	16
$C5	R	Rx Data 1	16
$C6	R	Status	16
$C7	W	Modem Control	16
$C8	W	Programming Register	16
$C9	R	Rx Data 2	16
$CA	W	Tx Data 1	16
$CB	W	Tx Data 2	16
$CC	R	Tone Status	16
$CD	W	Audio Tone	16
$CE	W	Interrupt Mask	16
$CF		Reserved	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

6.15.1 Interrupt Operation

The CMX7041 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the Status register, except the Programming Flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. The Programming Flag bit is set to 1 only when it is permissible to write a new word to the Programming register. See:

- Status – $C6 read
- Interrupt Mask - $CE write

6.15.2 General Notes

In normal operation, the most significant registers are:

- Mode Control – $C1 write
- Status – $C6 read
- Analogue Output Gain - $B0 write
- Input Gain and Output Signal Routing - $B1 write
- Audio Control – $C2 write

Setting the Mode register to either Rx or Tx will automatically increase the internal clock speed to its operational speed, whilst setting the Mode register to IDLE will automatically return the internal clock to a lower (powersaving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in IDLE mode.

Under normal circumstances the CMX7041 manages the Main Clock Control automatically, using the default values loaded in Program Block 3.

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	–0.3	4.5	V
AV_{DD}- AV_{SS}	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding V_{BIAS}) (i.e. V_{DEC}, AV_{DD}, AV_{SS}, DV_{DD} or DV_{SS})	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	668	mW
... Derating	–	6	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1410	mW
... Derating	–	14	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
DV_{DD} – DV_{SS}		3.0	3.6	V
AV_{DD} – AV_{SS}		3.0	3.6	V
V_{DEC} – DV_{SS}	12	2.25	2.75	V
Operating Temperature		–40	+85	°C
XTAL/CLK Frequency (using a Xtal)	11	4.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	11	4.0	24.576	MHz

Notes: 11 Nominal XTAL/CLK frequency is 6.144MHz.

12 The V_{DEC} supply is automatically created from DV_{DD} by the on-chip voltage regulator.

7.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 6.144MHz ±0.01% (100ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

Current consumption figures quoted in this section apply to the device when loaded with the current FI only. The use of other Function Images™, can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	8	100	µA
AI_{DD} (AV_{DD} = 3.3V)		–	4	20	µA
IDLE Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	1.1	TBD	mA
AI_{DD} (AV_{DD} = 3.3V)		–	35	TBD	µA
Rx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	3.4	TBD	mA
AI_{DD} (AV_{DD} = 3.3V)		–	1.5	TBD	mA
Tx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	3.4	TBD	mA
AI_{DD} (AV_{DD} = 3.3V)		–	1.5	TBD	mA
Additional current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	250	–	µA
Additional current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA

Notes:
21 Not including any current drawn from the device pins by external circuitry.
22 System Clocks, Auxiliary circuits, audio scrambler, compander and pre/de-emphasis disabled, but all other digital circuits (including the Main Clock PLL) enabled. A single analogue path is enabled through the device.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	23				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input current (Vin = DV_{DD})		–	–	40	µA
Input current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')		–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 120µA)		90%	–	–	DV_{DD}
(I_{OH} = 1mA)		80%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = 360µA)		–	–	10%	DV_{DD}
(I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
"Off" State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		–1.0	–	+1.0	µA
REPLY_DATA (output HiZ)		–1.0	–	+1.0	µA
V_{BIAS}	24				
Output voltage offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output impedance		–	22	–	kΩ

Notes: 23 Characteristics when driving the XTAL/CLK pin with an external clock source.

24 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' pulse width		31	15	–	–	ns
'Low' pulse width		31	15	–	–	ns
Input impedance (at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal start up (from powersave)			–	400	–	ms
Auxiliary System Clk 1/2 Outputs						
XTAL/CLK input to CLOCK_OUT timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' pulse width		33	76	81.38	87	ns
'Low' pulse width		33	76	81.38	87	ns
V_{BIAS}						
Start up time (from powersave)			–	30	–	ms
Microphone, Alternative and Discriminator Inputs (MIC, ALT, DISC)						
Input impedance		34	–	1	–	MΩ
Maximum Input Level (pk-pk)		35	–	–	80%	AV_{DD}
Load resistance (feedback pins)			80	–	–	kΩ
Amplifier open loop voltage gain (I/P = 1mV rms at 100Hz)			–	60	–	dB
Unity gain bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 6.144MHz XTAL fitted and 6.144MHz output selected.

34 With no external components connected

35 Centered about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DiscFB, AltFB OR MicFB

37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD 1, MOD 2, AUDIO)					
Power-up to output stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	–1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output current range (AV_{DD} = 3.3V)		–	–	±125	µA
Output voltage range	44	0.5	–	AV_{DD} –0.5	V
Load resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	–1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–1.0	0	+1.0	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output current range (AV_{DD} = 3.3V)		–	–	±125	µA
Output voltage range	44	0.5	–	AV_{DD} –0.5	V
Load resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centered about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion time	52	–	62.4	–	µs
Input impedance					
Resistance		–	10	–	MΩ
Capacitance		–	5	–	pF
Zero error (input offset to give ADC output = 0)		0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero error (output offset from a DAC input = 0)		0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centered about $AV_{DD}/2$.

7.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 6.144MHz ±0.01% (100ppm)); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.
All figures quoted in this section apply to the device when loaded with the current FI only. The use of other Function Images™, can modify the parametric performance of the device.

AC Parameters (cont.)		Notes	Min.	Typ.	Max.	Unit
Receiver Signal Type Identification						
Probability of correctly identifying signal type (SNR = 12dB)			–	>>99.9	–	%
CTCSS Detector						
Sensitivity	(Pure Tone)	71	–	–26	–	dB
Response Time	(Composite Signal)	72	–	140	250	ms
De-response Time	(Composite Signal)	72, 75	–	210	–	ms
Dropout immunity		75	–	160	–	ms
Frequency Range			60	–	260	Hz
IN-BAND TONE Detector						
Sensitivity	(Pure Tone)	73	–	–26	–	dB
Response Time	(Good Signal)		–	35	–	ms
De-response Time	(Good Signal)		–	–	45	ms
Drop-out immunity			–	–	20	ms
Frequency Range	(In-band tone)		400	–	3000	Hz
DCS Decoder						
Sensitivity		71	58	–	–	mVp-p
Bit-Rate Sync Time			–	2	–	edges
FFSK/MSK Decoder						
Signal Input Dynamic Range		74	100	–	800	mVrms
Bit Error Rate	(SNR = 20dB)	74	–	<1	–	10^{-8}
Receiver Synchronisation	(SNR = 12dB)					
Probability of bit 16 being correct			–	>99.9	–	%

Notes:

71 Sub-Audio Detection Level threshold set to 16mV.

72 Composite signal = 308mV rms at 1kHz + 75mV rms Noise + 31mV rms Sub-Audio signal. Noise bandwidth = 5kHz Band Limited Gaussian.

73 In-band Tone Detection Level threshold set to 16mV.

74 AV_{DD} = 3.3V, for a "101010101 ... 01" pattern measured at the input amplifier feedback pin. Signal level scales with AV_{DD}. See Figure 18 for variation of BER with SNR.

75 With sub-audio dropout time (P2.4) set to ≥ 120ms. The typical dropout immunity is approximately 40ms more than the programmed dropout immunity. The typical de-response time is approximately 90ms longer than the programmed dropout immunity. See section 8.2, P2.4 in the CMX7041 User Manual.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Audio Compandor					
Attack time		–	4.0	–	ms
Decay time		–	13	–	ms
0dB point	84	–	100	–	mVrms
Compression / Expansion ratio		–	2:1	–	
CTCSS Encoder					
Frequency Range		60.0	–	260	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	81	–1.0	0	+1.0	dB
Total Harmonic Distortion	82	–	2.0	4.0	%
In-Band Tone Encoder					
Frequency Range		400	–	3000	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	83	–1.0	0	+1.0	dB
Total Harmonic Distortion	82	–	2.0	4.0	%
DCS Encoder					
Bit Rate		–	134.4	–	bps
Amplitude Tolerance	81	–1.0	0	+1.0	dB
FFSK/MSK Encoder					
Output signal level		–	775	–	mVrms
Output level variation		–1.0	0	+1.0	dB
Output distortion		–	–	5	%
3rd harmonic distortion		–	–	3	%
Logic 1 freq 1200baud and 2400baud		1198	1200	1202	Hz
Logic 0 freq 1200baud		1798	1800	1802	Hz
2400baud		2398	2400	2402	Hz
Isochronous distortion (0 to 1 and 1 to 0)		–	–	40	µs

Notes:

81 AV_{DD} = 3.3V and Tx Sub-Audio Level set to 88mV p-p (31mV rms).

82 Measured at MOD 1 or MOD 2 output.

83 AV_{DD} = 3.3V and Tx Audio Level set to 871mV p-p (308mV rms).

84 AV_{DD} = 3.3V.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
Received **audio**	91	300	–	3000	Hz
12.5kHz channel transmitted **audio**	92	300	–	2550	Hz
25kHz channel transmitted **audio**	93	300	–	3000	Hz
Pass-band Gain (at 1.0kHz)		–	0	–	dB
Pass-band Ripple (wrt gain at 1.0kHz)		–2.0	0	+0.5	dB
Stop-band Attenuation		33.0	–	–	dB
Residual Hum and Noise	96	–	–50	–	dB
Pre-emphasis	94	–	+6	–	dB/oct
De-emphasis	95	–	–6	–	dB/oct
Audio Scrambler					
Inversion frequency		–	3300	–	Hz
Pass band		300	–	3000	Hz
Audio Expandor					
Input Signal Range	97	–	–	0.55	Vrms

Notes:

91 The receiver audio filter complies with the characteristic shown in Figure 7. The high pass filtering removes sub-audio components from the audio signal.

92 The 12.5kHz channel filter complies with the characteristic shown in Figure 10.

93 The 25kHz channel filter complies with the characteristic shown in Figure 9.

94 The pre-emphasis filter complies with the characteristic shown in Figure 11

95 The de-emphasis filter complies with the characteristic shown in Figure 8.

96 Measured in a 30kHz bandwidth.

97 AV_{DD} = 3.3V.

7.2 C-BUS Timing

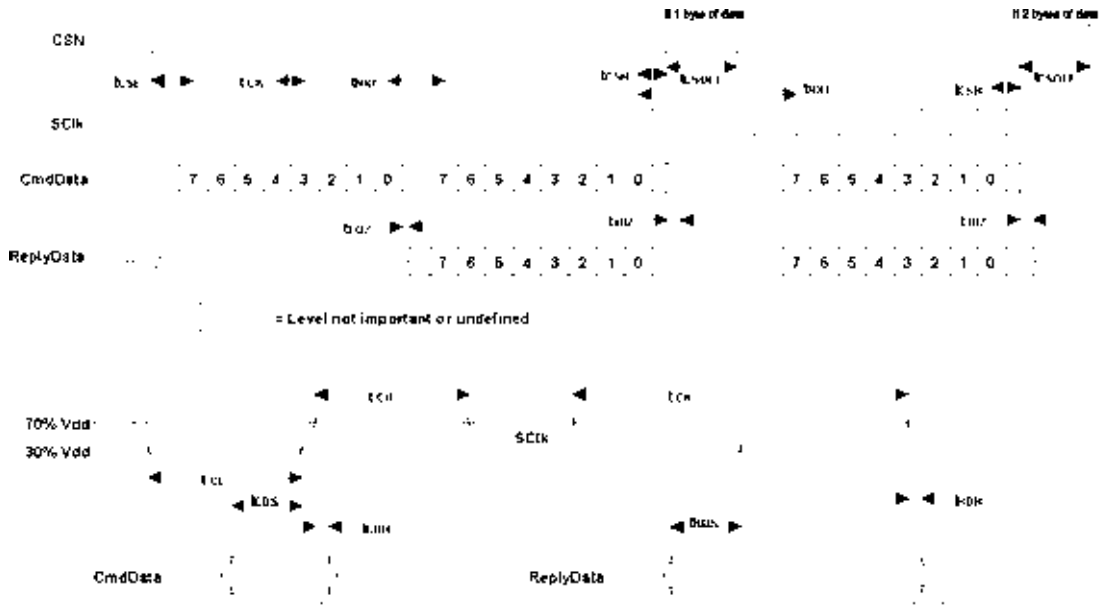


Figure 17 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SClk high time		100	–	–	ns
t_{CSH}	Last SClk high to CSN high time		100	–	–	ns
t_{LOZ}	SClk low to ReplyData Output Enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to ReplyData high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SClk cycle time		200	–	–	ns
t_{CH}	SClk high time		100	–	–	ns
t_{CL}	SClk low time		100	–	–	ns
t_{CDS}	Command Data setup time		75	–	–	ns
t_{CDH}	Command Data hold time		25	–	–	ns
t_{RDS}	Reply Data setup time		50	–	–	ns
t_{RDH}	Reply Data hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SERIAL_CLOCK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SERIAL_CLOCK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7041 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

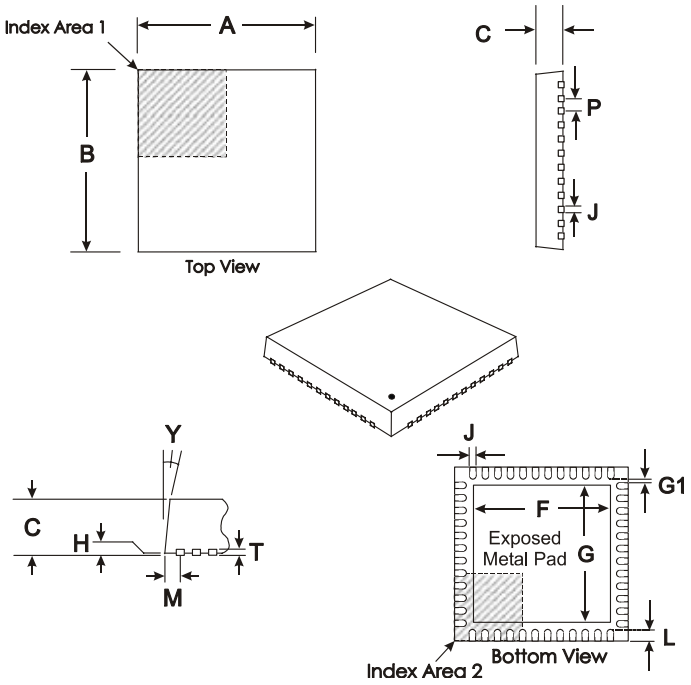
TBD

Figure 18 Typical FFSK/MSK Bit Error Rate Graph

TBD

Figure 19 Typical FFSK/MSK Block Error Rate Graph

7.3 Packaging

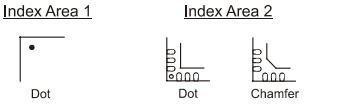


DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80		1.00
F	2.75		5.25
G	2.75		5.25
G1		0.225	
H	0.00		0.05
J	0.18		0.30
L	0.30		0.50
M		0.75	
P		0.50	
T		0.20	
Y	0°		12°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

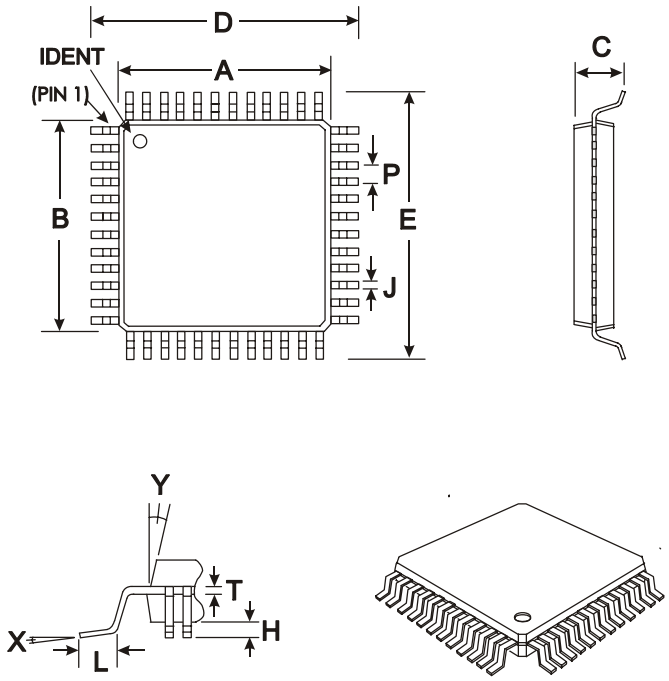
All dimensions in mm
Angles are in degrees



Index Area 1 is located directly above Index Area 2

Figure 20 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX7041Q3



DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 21 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX7041L4

About *FirmASIC*™

CML's proprietary *FirmASIC*™ component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*™ combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*™ device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*™ devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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CML Microcircuits

COMMUNICATION SEMICONDUCTORS

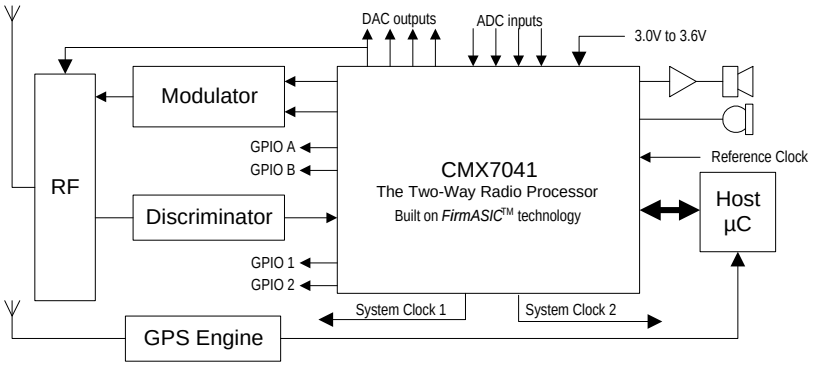
CMX7041
The Two-Way Radio Processor

UM/7041/1 February 2006 **USER MANUAL** Provisional Issue

CMX7041: Baseband Audio and Data Processor with System Clock O/P for Use in Analogue Radio Systems

Features

- **Concurrent Audio/Signalling/Data operations**
- **Full Audio-band Processing: Pre and De-emphasis, Compandor, Scrambler and Selectable 2.55 / 3 kHz Filters**
- **Inband Signalling: Selcall and DTMF**
- **2 x Auxiliary ADCs and 4 x Auxiliary DACs**
- **Low-power (3.0V to 3.6V) Operation**
- **C-BUS Serial Interface to Host µController**
- **3 x Analogue Inputs (Mic or Discriminator)**
- **FFSK/MSK Data Modem with Packet or Free-format modes with FEC, CRC, Interleaving and Scrambling**
- **Sub-Audio Signalling: CTCSS, DCS**
- **Auxiliary System Clock Outputs**
- **Tx Outputs for Single or Two Point Modulation**
- **Available in 48-pin LQFP and VQFN Packages**
- **Flexible Powersave Modes**



Brief Description

The CMX7041 is a full-function, half-duplex, audio, signalling and data processor IC. This makes it a suitable device for both the leisure radio markets (FRS, MURS, PMR446 and GMRS) and for professional radio products (PMR/LMR and Trunking) with or without signalling and data facilities.

The device utilises CML's proprietary *FirmASIC*™ component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external EEPROM or from a host µController over the built-in C-BUS serial interface. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

The CMX7041 features two programmable system clocks to minimise chip count in the final application.

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. . . . . continued

The device performs simultaneous processing of subaudio and inband signalling and audio band processing (including frequency inversion scrambling, companding and pre- or de-emphasis). Other features include a complete FFSK/MSK modem for packetised or free-format data, two Auxilliary ADC channels with four selectable inputs and up to four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping).

The device has flexible powersaving modes and is available in both LQFP and VQFN packages.

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

CONTENTS

It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

8 Configuration Guide

8.1 C-BUS Register Details

		hardware register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
01	w	reset																
A7	w	Aux ADC, TX mode	0	0	TX Mod mode		Aux ADC2 AV mode		AUX ADC2 ip select			Aux ADC1 AV mode		AUX ADC1 ip select			Ramp Up	Ramp Dn
A8	w	AuxDAC data/ena		0		RamDAC		DAC sel		AUX DAC data								
A9	r	AuxADC 1 data	Threshold status		x		x		x	AUX ADC 1 data								
	r	pon checksum 2 hi	power on checksum 2 hi															
AA	r	AuxADC 2 data	Threshold status		x		x		x	AUX ADC2 data								
	r	pon checksum 2 lo	power on checksum 2 lo															
AB	w	Sys Clk 1 PLL	System CLK 1 VCO divider								System CLK 1 Feedback divider							
AC	w	Sys Clk 1 Ref	IP sel	ENA clk	ENA div	bypass	IP sel	OP slew rate			Ref CLK 1 divider							
AD	w	Sys Clk 2 PLL	System CLK 2 VCO divider								System CLK 2 Feedback divider							
AE	w	Sys Clk 2 Ref	IP sel	ENA clk	ENA div	bypass	IP sel	OP slew rate			Ref CLK 2 divider							
AF	w	reserved																
B0	w	Analog Gain	INV	MOD1 gain		INV		MOD2 gain			0		0		0	AUDIO gain		
B1	w	Input routing	IP2 gain		IP1 gain				MD1 src		AUD	MD2	IP1 src		IP2 src		0	0
B2	w	reserved																
B3	w	reserved																
B4	w	reserved																
B5	w	Aux ADC threshold	ADC sel	Hi /Lo	0	0	0	0	Aux ADC threshold data									
B6	w	Modem Address	MSK Header Address						XTCSS Address									
B7	w	reserved																
B8	r	pon checksum 1 hi	power on checksum 1 hi															
B9	r	pon checksum 1 lo	power on checksum 1 lo															
BA	r	reserved																
BB	r	NWR data	NWR status			x	x	x	x	x	NWR SAME data							
BC	w	Main CLK PLL	Main CLK VCO divider							Main CLK Feedback divider								
BD	w	Main CLK Ref	IP sel	ENA clk	ENA div	IP sel	IP sel	IP sel	IP sel	Ref Main CLK divider								
BE	w	reserved																
BF	w	reserved																
C0	w	Power Down	ALT amp	MIC amp	DISC amp	IP gain	FineGain 1	FineGain 2	Gain 1	Gain 2	Audio OP	BIAS	RESET	Protect	XTAL DIS	0	0	Main DIS
C1	w	Mode Control	Voice mode		NWR		In-Band modes				Sub Audio mode			MSK mode		Idle / RX / TX		
C2	w	Audio Control	scramble	comp	emph	12k5	25k	hpf	sub audio modes		sub audio tone number: CTCSS / DCS / none							
C3	w	TX Tones	TX Inband Tone					0		0	0	twist	single	Tx DTMF tone				
C4	r	reserved																
C5	r	RX Data 1	RX Data 0								RX Data 1							
C6	r	Status	IRQ	NWR	RX in	xtcss	ctcss	dcs	Aux ADC2	Aux ADC1	FFSK	data	RXDT2	2k4	1k2	RXDT1	reserved	PRG
C7	w	Modem control	sync	synd	synt	En_NWR	0	type0	last	0	message format			Interleave	0	user bit	scramble seed	
C8	w	Programming	Program Block Address				Program Block Data											
C9	r	RX Data 2	RX Data 2 or XTCSS tone 3 and 2								RX Data 3 or XTCSS tone 1 and 0							
CA	w	TX Data 1	TX MSK data 0								TX MSK data 1							
CB	w	TX Data 2	TX MSK data 2 or XTCSS tone 3 and 2								TX MSK data 3							
CC	r	Tone Status	Selcall Tone detected				Sub Audio status				Sub Audio Tone detected							
CD	w	Audio Tone	0	0	0	0	Audio Tone Frequency											
CE	w	Interrupt Mask	IRQ	NWR	RX Inband	XTCSS	CTCSS	DCS	Aux ADC2	Aux ADC1	FFSK	Data RDY	Data CRC	2k4	1k2	reserved	reserved	PRG
CF	w	reserved																

The detailed descriptions of the C-BUS registers are presented in numerical order and should be read in conjunction with the relevant functional descriptions.

8.1.1 Reset Operations

A reset is automatically performed when power is applied to the CMX7041. A reset can be issued as a C-BUS command, either as a General Reset command ($01), or by setting the appropriate bit (b5) in the Powerdown Control register ($C0). In the latter case, an option exists to protect the values held in the Program Block (which is accessed via the Programming register, $C8). The action of each reset type is shown in the table below:

Table 13 Reset Operations

	Reset type	BOOTEN pins (2, 1)	FI load Block 1 and 2	FI load Activation Block	Protect bit ($C0 b4) state	Activation Code	Program Block state
1	Power on	11	required	required	cleared by h/w	required	default
2	General Reset (C-BUS $01)	11	optional	required	cleared by h/w	required	default
3	General Reset (C-BUS $01)	00	no	no	cleared by h/w	required	default
4	Reset (C-BUS $C0 b5)	11	optional	required	0	required	default
5	Reset (C-BUS $C0 b5)	11	optional	required	1	no	protected
6	Reset (C-BUS $C0 b5)	00	no	no	0	required	default
7	Reset (C-BUS $C0 b5)	00	no	no	1	no	protected

Notes:
The Protect bit (C-BUS register $C0 b4) should NOT be set to 1 during an FI load.

8.1.2 General Reset - $01 write

The General Reset command has no data attached to it. It puts the device registers into the states listed below. A power-on reset performs the same action.

ADDR.	REGISTER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$A7	AuxADC / TX Mode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A8	AuxDAC data/enable	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A9	AuxADC 1 data *power-on checksum 2 hi*	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
$AA	AuxADC 2 data *power-on checksum 2 lo*	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
$AB	System Clk 1 PLL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$AC	System Clk 1 Ref	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$AD	System Clk 2 PLL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$AE	System Clk 2 Ref	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$AF	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B0	Analog Gain	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B1	Input Routing	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B2	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B3	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B4	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B5	Aux ADC Threshold	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B6	Modem Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B8	*power-on checksum 1 hi*	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
$B9	*power-on checksum 1 lo*	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
$BB	NWR data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$BC	Main CLK PLL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$BD	Main CLK Ref	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$BE	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$BF	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C0	Power Down	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C1	Mode Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C2	Audio Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C3	TX Tones	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C5	RX Data 1 *product identification*	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
$C6	Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C7	Modem Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C8	Programming	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C9	RX Data 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CA	TX Data 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CB	TX Data 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CC	Tone Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CD	Audio Tone	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CE	Interrupt Mask	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CF	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Notes: 'c' is the power-on checksum or product identification, returned in registers $A9, $AA, $B8, $B9 and $C5. Any registers not mentioned above are undefined. The BOOTEN pins MUST be set to an appropriate state before and during any reset (see Table 13). After a General Reset, or after a new FI has been loaded, the Device Activation code will need to be sent before the CMX7041 exhibits any functionality.

8.1.3 AuxADC and TX MOD mode - $A7 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Tx Mod mode		Aux ADC2 AV mode		AUX ADC2 ip select			Aux ADC1 AV mode		AUX ADC1 ip select			RU	RD

b15 reserved, clear to 0
b14 reserved, clear to 0

		Tx MOD mode	
b13	**b12**	**OUTPUT1**	**OUTPUT2**
1	1	In-Band + Sub-Audio	In-Band + Sub-Audio
1	0	In-Band + Sub-Audio	Sub-Audio
0	1	In-Band	Sub-Audio
0	0	bias	bias

To select the routing between the OUTPUT1, OUTPUT2 and MOD 1, MOD 2 and Audio, see section 8.1.10

		AuxADC Averaging Mode
b11	**b10**	**AuxADC2**
b6	**b5**	**AuxADC1**
1	1	reserved
1	0	reserved
0	1	rolling average, uses Program Block 3.0 value
0	0	No averaging

			AuxADC Input Select
b9	**b8**	**b7**	**AuxADC2**
b4	**b3**	**b2**	**AuxADC1**
1	1	1	Aux4
1	1	0	Aux3
1	0	1	Aux2
1	0	0	Aux1
0	1	1	MIC
0	1	0	ALT
0	0	1	DISC
0	0	0	off

b1 Ramp Up enable 0 = off 1 = on
b0 Ramp Down enable 0 = off 1 = on

When bits 1 or 0 are set to '1' the MOD output signals are ramped to reduce transients in the transmitted signal. The ramp up / down time is set in the 'Ramp Rate Control' section of the Programming register (P4.6).

8.1.4 AuxDAC control / data - $A8 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA	0	0	Ram DAC	DAC sel		AUX DAC data									

b15 enable selected Aux DAC 0 = disable 1 = enable
b14 reserved
b13 reserved
b12 RAMDAC enable 0 = AuxDAC1 operates normally
1 = AuxDAC1 operates as a RAMDAC[1]. Data in b0-6 controls the RAMDAC functions.

b11, b10 select the AuxDAC that b9-b0 data will be written to
00 = AuxDAC1
01 = AuxDAC2
10 = AuxDAC3
11 = AuxDAC4
b9 – b0 AuxDAC data (unsigned)

Note: when $A8 b12 is set to 1, writing data to this register controls the RAMDAC settings. Writing to AuxDAC1 with this bit set may cause un-intended operation whilst the RAMDAC is ramping. In this mode b9 to b0 perform the following functions:

b9 reserved, clear to 0
b8 reserved, clear to 0
b7 reserved, clear to 0
b6 RAMDAC RAM access, 0 resets the internal RAMDAC address pointer

			RAMDAC scan time	
b5	b4	b3	divider	time(ms)
0	0	0	1024	10.50
0	0	1	512	5.25
0	1	0	256	2.63
0	1	1	128	1.31
1	0	0	64	0.66
1	0	1	32	0.33
1	1	0	16	0.16
1	1	1	8	0.08

b2 Scan direction: 0 = ramp down 1 = ramp up
b1 Autocycle 0 = disable 1 = continuous ramp up/down
b0 RAMDAC start 0 = stop 1 = start RAMDAC ramping

To initiate a RAMDAC ramp up write: $9005
To initiate a RAMDAC ramp down, write: $9001

Note that initiating a RAMDAC scan will automatically bring AuxDAC1 out of powersave. To place AuxDAC1 back into powersave, it must be written to explicitly. Do NOT change IDLE / Rx / Tx mode whilst the RAMDAC is still ramping.

[1] Do NOT write to directly to AuxDAC 1 whilst the RAMDAC is in operation. RAMDAC is only available when in Tx mode.

8.1.5 AuxADC1 data - $A9 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold status		x	x	x	x	AUX ADC 1 data									

b15, b14 threshold status

b15 = 1 signal is above the high threshold
= 0 signal is below the high threshold
b14 = 1 signal is below the low threshold
= 0 signal is above the low threshold

b13 reserved
b12 reserved
b11 reserved
b10 reserved
b9 –b0 AuxADC1 data or last reading (unsigned)

8.1.6 AuxADC2 data - $AA read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold status		x	x	x	x	AUX ADC 2 data									

b15, b14 threshold status

b15 = 1 signal is above the high threshold
= 0 signal is below the high threshold
b14 = 1 signal is below the low threshold
= 0 signal is above the low threshold

b13 reserved
b12 reserved
b11 reserved
b10 reserved
b9 –b0 AuxADC2 data or last reading (unsigned)

8.1.7 System CLK 1 and 2 PLL data - $AB, $AD write
C-BUS address: $AB – System Clk 1 PLL
C-BUS address: $AD – System Clk 2 PLL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCO Op divide ratio <5-0>						PLL feedback divide ratio <9-0>									

b15-b10 divide the selected output clock source by the value in these bits, to generate the System Clk output. Divide by 64 is selected by setting these bits to '0'.

b9-b0 divide System Clk PLL VCO clock by value set in these bits as feedback to the PLL phase detector (PD); when the PLL is stable, this will be the same frequency as the internal reference as set by b8-b0 of the System Clk Reference and Source Configuration register ($AC). Divide by 1024 is selected by setting these bits to '0'.

8.1.8 System CLK 1 and 2 REF - $AC and $AE write
C-BUS address: $AC – System Clk 1 Ref
C-BUS address: $AE – System Clk 2 Ref

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Select & PS Clock Sources					op slew		Ref Clock divide ratio <8-0>								

b15,12,11 Clk output divider source

Sys CLK 1 Source	B15	B12	B11
Xtal	0	X	X
Sys Clk PLL 1	1	0	0
Main PLL	1	0	1
Test	1	1	X

Sys CLK 2 Source	B15	B12	B11
Xtal	0	X	X
Sys Clk PLL 2	1	0	0
Main PLL	1	0	1
Sys Clk PLL 1	1	1	0
Test	1	1	1

b14 Powersave PLL 0 = powersave 1 = enabled
b13 Powersave Output Divider 0 = powersave 1 = enabled
b10-9 Output Slew Rate

b10	b9	Output Slew Rate
0	0	normal
0	1	slow
1	0	fast
1	1	fast

b8-b0 Reference Clk divide value. Divide by 512 is selected by setting these bits to '0'.

Note that after a General Reset, the default setting (b13 = 0) will not provide any clock output on the SYSCLOCK1 and SYSCLOCK2 pins. These pins will be connected to '0'.

8.1.9 Analogue Output Gain - $B0 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Inv_1	MOD 1 Attenuation			Inv_2	MOD 2 Attenuation			0	0	0	0	Audio Output Attenuation			

b15 MOD1 output polarity 0 = true 1 = inverted

b11 MOD2 output polarity 0 = true 1 = inverted

Used when interfacing with RF circuitry or when generating an inverted turn-off code for CTCSS. Any change will take place immediately (within the C-BUS latency period) after these bits are changed.

b14	b13	b12	MOD 1 Output Attenuation
b10	**b9**	**b8**	**MOD 2 Output Attenuation**
0	0	0	>40dB
0	0	1	12dB
0	1	0	10dB
0	1	1	8dB
1	0	0	6dB
1	0	1	4dB
1	1	0	2dB
1	1	1	0dB

Bits 7 to 4 are reserved - set to 0.

b3	b2	b1	b0	Audio Output Attenuation
0	0	0	0	>60dB
0	0	0	1	44.8dB
0	0	1	0	41.6dB
0	0	1	1	38.4dB
0	1	0	0	35.2dB
0	1	0	1	32.0dB
0	1	1	0	28.8dB
0	1	1	1	25.6dB
1	0	0	0	22.4dB
1	0	0	1	19.2dB
1	0	1	0	16.0dB
1	0	1	1	12.8dB
1	1	0	0	9.6dB
1	1	0	1	6.4dB
1	1	1	0	3.2dB
1	1	1	1	0dB

Note that Fine level control of Output 1 and Output 2 can be achieved with the FINE OUTPUT GAIN 1 and FINE OUTPUT GAIN 2 registers (P4.2-3). These affect the MOD 1, MOD 2 and AUDIO outputs according to the routing set in registers $A7 and $B1

8.1.10 Input Gain and Output Signal Routing - $B1 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Input 2 Gain			Input 1 Gain			MOD 1 source		MOD 2	AUDIO Source	Input 1 routing		Input 2 routing		0	0

b12	b11	b10	Input 1 Gain
b15	**b14**	**b13**	**Input 2 Gain**
0	0	0	0dB
0	0	1	3.2dB
0	1	0	6.4dB
0	1	1	9.6dB
1	0	0	12.8dB
1	0	1	16.0dB
1	1	0	19.2dB
1	1	1	22.4dB

b7	MOD 2 Source
0	bias -> MOD 2
1	Output 2 -> MOD 2

b6	Audio Source
0	bias -> Audio
1	Output 1 -> Audio

b9	b8	MOD 1 Signal Routing
0	0	bias
0	1	bias
1	0	Output 1 -> MOD 1
1	1	Output 2 -> MOD 1

b5	b4	Input 1 Signal Routing
b3	**b2**	**Input 2 Signal Routing**
0	0	bias
0	1	Disc
1	0	Alt
1	1	Mic.

Output1 and Output 2 signal sources are also defined in section 8.1.3.

Bits 1, 0 are reserved – clear to '0'.

In normal operation, all signal processing blocks would be set to work with Input Signal 1. There are a number of applications where it may be desirable to split the processing across both inputs. Such applications could be monitoring two RF receivers, or where an external voice encryption unit is required which does not pass Sub-Audio signalling in Rx (in which case, Input Signal1 could be routed to the DISC input with voice and in-band processing set to Input Signal 2 on the ALT input).

Similarly, for the Output routing, under normal operation, Output 1 would be routed to MOD 1 and Output 2 to MOD 2. The signals that appear on Output 1 and Output 2 are defined in b13, b12 in $A7.

8.1.11 AuxADC threshold data - $B5 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC sel	Hi /Lo	0	0	0	0	Aux ADC threshold data									

b15 AuxADC select 0 = AuxADC1 1 = AuxADC2
b14 high / low select 0 = low threshold 1 = high threshold
b13 reserved 0
b12 reserved 0
b11 reserved 0
b10 reserved 0
b9 –b0 threshold data

8.1.12 Modem Address - $B6 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK Header Address								XTCSS Address							

b15 – 8 MSK Header Address
b7 – 0 XTCSS Address

8.1.13 Main CLK PLL - $BC write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCO Op divide ratio <5-0>						PLL feedback divide ratio <9-0>									

b15-b10 divide the selected clock source (Main Pre Clk) by the value in these bits, to generate the Main Clk output. Divide by 64 is selected by setting these bits to '0'.
b9-b0 divide Main VCO Clk by value set in these bits as feedback to the PLL phase detector (PD); when the PLL is stable, this will be the same frequency as the internal reference as set by b8-b0 of the Main Clk Reference and Source Configuration register ($BD). Divide by 1024 is selected by setting these bits to '0'.

8.1.14 Main CLK Reference and Source Configuration - $BD write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Select/PS Main Clk			0				Ref Clock divide ratio <8-0>								

b15 Select Main Pre Clk Source 0 = Xtal Reference Clock 1 = Main VCO Clock
b14 Powersave Main Clk PLL 0 = powersave 1 = enabled
b13 Powersave Output Divider 0 = powersave / bypass 1 = enabled
b12-9 set these bits to '0'
b8-b0 Main Reference Clk divide value. Divide by 512 is selected by setting these bits to '0'.

8.1.15 NWR status and data - $BB read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NWR status			x	x	x	x	x	NWR SAME data							

b15 NWR WAT tone status 0 = no tone 1 = WAT tone detected
b14 NWR SAME synch status 0 = no synch 1 = synch detected
b13 NWR SAME data status 0 = no data 1 = data detected
b12 reserved
b11 reserved
b10 reserved
b9 reserved
b8 reserved
b7 – 0 NWR SAME data

8.1.16 Power Down Control - $C0 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALT amp	MIC amp	DISC amp	IP1 ENA	OP1 ENA	OP2 ENA	MOD1 ENA	MOD2 ENA	Audio OP	BIAS	Reset	Protect	XTAL DIS	IP2 ENA	0	0

b15 ALT amp enable 0 = off 1 = enabled
b14 MIC amp enable 0 = off 1 = enabled
b13 DISC amp enable 0 = off 1 = enabled
b12 Input 1 enable 0 = off 1 = enabled
b11 Output 1 enable 0 = off 1 = enabled
b10 Output 2 enable 0 = off 1 = enabled
b9 MOD 1 enable 0 = off 1 = enabled

b8	MOD 2 enable	0 = off	1 = enabled
b7	Audio Output enable	0 = off	1 = enabled
b6	BIAS block enable	0 = off	1 = enabled
b5	Reset	0 = normal	1 = reset / powersave
b4	Program Block Protect	0 = normal	1 = protected

If cleared, the Program Blocks will be initialised on Power on or Reset. If set, then the Program Blocks will retain their previous contents.

b3	XTAL disable	0 = enabled	1 = disabled / powersave

Setting this bit effectively stops all signal processing within the device.

b2	Input 2 enable	0 = off	1 = enabled
b1	reserved	0	1 = DO NOT USE
b0	reserved	0	1 = DO NOT USE

Note: Care should be taken when writing to b5 and b3. These are automatically programmed to an operational state following a power-on (ie: all 0's). Writing a 1 to either b5 or b3 will effectively cause the device to cease all processing activity, including responding to other C-BUS commands (except General Reset, $01).

When b5 is set, the device will be held in reset and all signal processing will cease (including AuxADC operation); when subsequently cleared to 0, the BOOTEN pins will be read and the appropriate boot mode executed. In the Host Load configuration, if the FI is unchanged and the power supplies have remained stable during the reset period, it is permissible to leave the BOOTEN pins in the Host Load state and send only the Activation Block rather than the full FI to the device. Otherwise, the BOOTEN pins should be set to the "No FI Load" state BEFORE clearing the Reset.

When b3 is set the Xtal is disabled. When b3 is subsequently cleared, it may take some time for the clock signal to become stable, hence care should be taken in using this feature.

8.1.17 Mode Control – $C1 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Audio mode		NWR		In-Band modes				Sub Audio mode			MSK mode			Idle / Rx / Tx	

b15	Audio processing source	0 = Input1	1 = Input2
b14	Audio processing enable	0 = off	1 = enabled
b13	NWR processing source	0 = Input1	1 = Input2
b12	NWR processing enable	0 = off	1 = enabled
b11	In-Band Processing source	0 = Input1	1 = Input2

b10	b9	b8	In Band Processing Mode
1	1	1	Reserved
1	1	0	Reserved
1	0	1	Reserved
1	0	0	Audio Tones
0	1	1	Reserved
0	1	0	Selcall
0	0	1	DTMF (Tx only)
0	0	0	off

b7	Sub-Audio Processing source	0 = Input1	1 = Input2
b6	CTCSS enable	0 = off	1 = enabled
b5	DCS enable	0 = off	1 = enabled
b4	MSK processing source	0 = Input1	1 = Input2
b3	MSK 2400 enable	0 = off	1 = enabled
b2	MSK 1200 enable	0 = off	1 = enabled

b1, b0	Operational mode	00	IDLE
		01	Rx
		10	Tx
		11	reserved

Changes to the settings of the bits in this register are implemented as soon as they are received over the C-BUS (note that the C-BUS has a potential latency of up to 250µs).

In Tx mode, it is not permissible to set BOTH b3 and b2 at the same time.
In Tx mode, it is only permissible to select ONE of the following at any time:

Audio
In-Band Signalling
MSK / FFSK data

It is essential that changes to the Program Register and the Audio Control register are completed before entering Rx or Tx mode.

The following other registers or bits can be changed as appropriate (Note: not all possible changes are appropriate), whilst the device is in Tx or Rx mode:

- Analogue Output Gain register ($B0)
- Input Gain and Signal Routing register ($A7)
- Input Gain and Signal Routing (2) register ($B1)
- Power Down Control register ($C0)
- Tx Inband Tones register ($C3)
- Modem Control register ($C7) bit 9 only, as described in section 6.8
- Tx Data registers ($CA & $CB)
- Audio Tone register ($CD)
- Interrupt Mask register ($CE)

In Rx mode, as certain FFSK bit patterns can mimic In-band tones, the In-band receiver is temporarily disabled when an FFSK frame sync is detected. If using sized packets (type 1, 4 and 5) the CMX7041 will automatically restore In-band tone detection when the received message has ended. If using unsized packets (type 0, 2 and 3) the host must monitor the received data and restore XTCSS / In-band tones (by setting bits 14 and 13 as required) when it has detected the end of data.

8.1.18 Audio Control – $C2 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
scra-mble	comp	emph	12k5	25k	hpf	sub audio modes		sub audio tone number: CTCSS / DCS / none							

b15	Audio Scrambling enable	0 = off	1 = enabled
b14	Audio Compandor enable	0 = off	1 = enabled
b13	Audio Pre / De-emphasis	0 = off	1 = enabled[2]
b12	Audio 12.5kHz Filter enable	0 = off	1 = enabled
b11	Audio 25kHz Filter enable	0 = off	1 = enabled
b10	Audio 300Hz HPF enable	0 = off	1 = enabled

b9, b8	CTCSS phase	00	0 degrees (normal)
		01	120 degrees
		10	180 degrees
		11	240 degrees

b7 – b0	Sub-Audio Tone number (dec)	0	no tone
		1 to 83	select DCS code 1 to 83
		84	select User Defined DCS code
		101 to 183	select DCS tone 1 to 83 inverted
		184	select User Defined DCS code inverted
		200	select Tone Clone™ mode
		201 to 251	select CTCSS tone 1 to 51
		252	select User Defined CTCSS tone
		253	select XTCSS maintenance tone
		254	select DCS turn-off tone
		255	Invalid tone

Selecting the 'DCS turn-off tone (254)' during DCS transmit will cause the DCS turn off tone to be transmitted. CTCSS does not need to be enabled in the Mode Control register to receive the 'DCS turn off tone'.

To transmit the 64.7Hz XTCSS maintenance tone, XTCSS and CTCSS transmit must be selected in the Mode Control register and this register set to 253 decimal. Transmission of the maintenance tone overrides any other CTCSS tone being transmitted. The XTCSS maintenance tone decoder is enabled by selecting CTCSS receive modes in the Mode Control register and tone 253 in this register.

If the Tone Clone™ mode is selected this allows the device in Rx to non-predictively detect any CTCSS frequency in the range of valid tones, the received tone number will be reported in the Tone Status register ($CC) and the CTCSS decoder detection bandwidth should be set to its lowest value (P2.1)

8.1.19 Tx In-band Tones - $C3 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tx In-band tone					0	0	0	0	0	twist	sgl	Tx DTMF tone			

b15-11	User or Selcall Tone, see Table 6 In-band Tones		
b10-6	reserved, clear to '0'.		
b5	DTMF Twist	0 = normal	1 = -2dB of twist applied to the lower DTMF tone.
b4	DTMF Single Tone	0 = normal	1 = Single Tone, see Table 7 DTMF Tone Pairs
b3-0	DTMF tone value – see Table 7 DTMF Tone Pairs		

8.1.20 Rx Data 1 - $C5 read

See section 6.8.1 and 8.1.24.

[2] In order to pre-emphasise the MSK data, Program Block P1.0 bit 0 should be set.

8.1.21 Status – $C6 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	NWR	Rx in	xtcss	Ctcss	dcs	Aux ADC2	Aux ADC1	FFSK	Data RDY	Data CRC	2k4	1k2	res	res	PRG

b15 IRQ

Changes in the Status register will cause this bit to be set to 1 if the corresponding interrupt mask bit is enabled. An interrupt request is issued on the IRQN pin when this bit is 1 and the IRQ MASK bit (b15 of Interrupt Mask register, $CE) is set to 1.

b14 NWR status change

The NOAA Weather Receiver has detected a change in the status of the WAT tone or SAME data. The NWR data / status register $BB should be read to determine the exact cause.

b13 In-Band Tone event

The Tone Status register $CC should be read to determine the exact cause. Cleared to 0 in Tx.

b12 XTCSS event

A valid XTCSS four-tone set has been detected. The four received tones are indicated in the XTCSS register ($C9). In Tx, this bit will be set to 1 at the end of the 4th XTCSS tone transmitted.

b11 CTCSS event

A CTCSS code has been detected or ceased. The Tone Status register $CC should be read to determine the exact cause. Cleared to 0 in Tx.

b10 DCS event

A DCS code has been detected or ceased. The Tone Status register $CC should be read to determine the exact cause. Cleared to 0 in Tx.

b9 AuxADC2 Threshold change

AUX ADC2 signal has just gone above the high threshold or has just gone below the low threshold. The AuxADC2 data register $AA should be read to determine the exact cause.

b8 AuxADC1 Threshold change

AUX ADC1 signal has just gone above the high threshold or has just gone below the low threshold The AuxADC1 data register $A9 should be read to determine the exact cause.

b7 FFSK Data Complete

Rx mode: this is only valid when bit 6 'Data Ready' is set. It is set when receiving the last part of a sized FFSK Frame or Type 1 (frame head only) message, bit 5 (CRC) will also be updated at this time. When the host detects bit 7 is set it may power down the CMX7041 or set the CMX7041 to transmit or receive new information as appropriate.

Tx mode: this will be set when the last bit of FFSK/MSK data has been transmitted. Note; when using type 0, 2 or 3 data formats (see section 6.9) this bit will only be set if bit 9 of the Modem Control register ($C7) is set at the appropriate time. After allowing a short time delay associated with the external components and radio circuitry, the host may power down the CMX7041 and transmitter or set the CMX7041 to transmit or receive new information as appropriate.

b6 Data Ready

Tx mode: indicates that new transmit data is required.

Rx mode: received data is ready to be read.

For continuous transmission or reception of information, a data transfer should be completed within the time appropriate for that data (see Table 11).

b5 Data CRC received

Bit 5 will be set after receiving a correct CRC portion of a sized Data Block (types 4 and 5).

b4 2400 FSK data received

b3 1200 MSK data received

Bits 4 and 3 indicate the received data rate after a valid data sequence has been received. If data Type 0 formatting is enabled these bits will be set on detection of a valid frame sync pattern. If Type 0 formatting is disabled then these bits will only be set when a Frame Head is detected with a correct CRC.

b2 reserved for future use.

b1 reserved for future use.
b0 Program Register Ready
When set to 1, this bit indicates that the Program Register, $C8 is available for the host to write to it. Cleared by writing to the Programming Register, $C8

Bits 2 to 15 of the Status register are cleared to '0' after the Status register is read. Detection of the DCS turn off tone and removal of the DCS turn off tone are both flagged as DCS events in the Status register, not as CTCSS events. The assertion or removal of the 'XTCSS Maintenance Tone' (64.7Hz) is flagged as a CTCSS event.

The data in this register is not valid if bit 5 of the Power Down Control register, $C0 is set to 0.

8.1.22 Modem Control - $C7 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SynC	SynD	SynT	En_nwr	0	Type 0 format	Last Tx data	0	MSK message format			0	0	User bit	Scramble seed	

This register configures the way the CMX7041 handles MSK data in Tx and Rx modes.

b15 MSK Rx SynC detect 0 = off 1 = enabled
b14 MSK Rx SynD detect 0 = off 1 = enabled
b13 MSK Rx SynT detect 0 = off 1 = enabled
note: SynC, SynD and SynT patterns are defined in Program registers P0.0-3
b12 NWR data reception 0 – disabled 1 enabled
The en_NWR bit is required to control the actions of the NWR SAME data decoder. While the decoder can detect and respond to the arrival of a synch signal, it does not not know when the SAME transmission has ceased. The host will need to decode the data from the CMX7041, recognise the end of frame marker and then disable the SAME decoder through bit 12.
b11 reserved, clear to '0'.
b10 raw data mode: 0 = data packetizing on 1 = raw data mode
Receive mode:
b10 = '1': device will look for the programmed Frame Sync. pattern, raise an interrupt (if enabled) and decode the following data 16 bits at a time, making them available in Rx Data 1 register ($C5).
b10 = '0': device will look for a complete Frame Head before raising an interrupt (if enabled) and then decode the following data in accordance with the received message format. The Frame Head Control Field bytes, User Data and any CRC will be presented in the appropriate Rx Data registers ($C5 and $C9).
Transmit mode:
b10 = '1': device will transmit data 16 bits at a time from Tx Data 1 register ($CA). Bit and frame sync pattern generation and all formatting of the data have to be performed by the host in this case.
b10 = '0': device will transmit the programmed bit and frame sync patterns followed by a Frame Head containing the information supplied in bits 7–0 of this register and the 2 bytes in Tx Data 1 register ($CA). Subsequently the host must supply data when requested to complete the transmission of the data packet as defined in the Frame Head bytes.
b9 is only valid when transmitting data with type 0, 2 or 3 formatting and indicates to the CMX7041 that it can cease modulation. The host must set this bit to '1' immediately after the interrupt for 'load more data' occurs ($C6 bit 6). In receive, or when transmitting other message formats, this bit must be cleared to '0'.
b8 reserved, clear to '0'.

b7-5 data format:

b7	b6	b5	Type	**Message Format**
0	0	1	1	Frame Head only, no payload
0	1	0	2	Frame Head + Unsized payload of raw 16 bit words
0	1	1	3	Frame Head + Unsized payload with FEC
1	0	0	4	Frame Head + Sized payload with FEC + CRC
1	0	1	5	Frame Head + Sized payload with FEC + CRC + interleaving
All other patterns			-	Reserved

b4 Frame Head Interleave 0 = off 1 = on

b3 reserved, clear to '0'.

b2 User bit. May be freely used by the host. This bit has no effect on the message format or encoding and will be reported in the Rx Data 1 register for the receiving host to use as appropriate. This bit could be used to indicate a special message, e.g. one containing handset or channel set-up information.

b1-0 Scrambler Seed Select. Used when transmitting User Data. The receiving CMX7041 will automatically de-scramble the received User Data using the setting indicated in the received Frame Head. The receiving host can read the scrambler setting (0-3) used by the transmitter via Rx Data 2 register ($C9) and may use this when returning messages. See also section 6.9.5.

Bit 1	Bit 0	**MSK data scrambling setting:**
0	0	Standard scrambling (seed = $FFFF)
0	1	Scramble Seed1 (see P0.2-3)
1	0	Scramble Seed2 (see P0.4-5)
1	1	No scrambling (seed = $0000)

8.1.23 Programming Register – $C8 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Program Block Address				Program Block Data											

See section 8.2 for a definition of programming block operation.

8.1.24 Rx Data 2 and XTCSS - $C9 read

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$C5	Rx Data Byte 0 (Frame Head: Address byte)								Rx Data Byte 1 (Frame Head: Format byte)							
$C9	Rx Data Byte 2* (Frame Head: Size / Information byte)								Rx Data Byte 3* (Frame Head: CRC byte)							
	XTCSS Tone 3 (S1)				XTCSS Tone 2 (S0)				XTCSS received address							

*$C9 is used when receiving Type 4 and 5 formats and Frame Heads, the Rx buffer is effectively 4 bytes long in these cases.

These 2 words hold the most recent 2 bytes (Byte 0 and 1) or 4 bytes (Bytes 0, 1, 2 and 3) of MSK data decoded. Received data is continuous, if the data is not read before the next data is received the current data will be over-written.

XTCSS register ($C9) holds the information decoded after receiving an XTCSS type tone set. Bits 7 to 0 represent the received address in hex, based on the XTCSS tones A1 and A0. This register will only be updated if the received address matches the one programmed in the Audio Control register ($C2) or is the all call address of '40'. Bits 15 to 12 and 11 to 8 defines the received S1 and S0 tones, see Table 6 and section 5.7.

Although XTCSS register ($C9) holds both Rx data and Rx XTCSS tone information, only one type of signal will be present in the received signal at any one time so no conflict will occur.

After receiving a Frame Head the host can read the Address and Size / Information bytes for the following packet from Rx Data #1 register ($C5) and optionally the Control byte and the Frame Head Checksum A byte from Rx Data #2 register ($C9). The CMX7041 will read the Size and Message formatting information and if the message is of type 3, 4 or 5 (see section 6.9), it will start the automatic decoding of the following data; descrambling, de-interleaving, decoding error correction bytes, stripping out pad bytes, calculating and checking Checksum B as required. The only task the host need perform during the reception of formatted Frames is to read out data when it is ready.

8.1.25 XTCSS and Tx Data 1 and 2 - $CA and CB write

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$CA	Tx MSK Data Byte 0 (Frame Head: Address byte)								Tx MSK Data Byte 1 (Frame Head: Size / Information byte)							
$CB*	Tx Data Byte 2*								Tx Data Byte 3*							
	XTCSS Tone 3 (S1)				XTCSS Tone 2 (S0)				0	0	0	0	0	0	0	0

*Register $CB is only used for Type 4 and 5 data formats and Frame Heads, the Tx buffer is effectively 4 bytes long in these cases.

These 2 words hold next 2 bytes (Byte 0 and 1) or 4 bytes (Bytes 0, 1, 2 and 3) of MSK data to be transmitted. Outgoing data is continuous, if new data is not provided before the current data has been transmitted the current data will be re-transmitted, until new data is provided. Transmission of current data will be completed before transmission of newly loaded data begins. See section 6.8.2.

Tx Data #2 register ($CB) holds the codes to be used when transmitting an XTCSS type tone set. Each 4 bits define the In-band tone used, see Table 6 In-band Tones. S0 and S1 are the information section of the 4-tone set. This register must be set to the required value before XTCSS transmission is enabled. For more details see section 5.7. Note: The XTCSS address used is defined in the Audio and Device Address Control register.

Although Tx Data #2 register ($CB) holds both Tx data and Tx XTCSS tone information, these functions can not be used simultaneously so no conflict will occur.

When transmitting formatted MSK data packets, the host must first load the correct Address and Size / Information bytes for the following packet into Tx Data #1 register ($CA). The CMX7041 will automatically

add the Control byte, based on the settings in Modem Control register ($C7), and calculate the Frame Head Checksum A byte. The CMX7041 will read the Size and Message formatting information and automatically format all following data; adding error correction bytes, adding pad bytes, interleaving, scrambling and calculating and appending Checksum B as required. The only task the host need perform during the transmission of a Frame is to download new data when it is required.

Note: These 2 words must be written separately. i.e. Two 16 bit C-BUS transactions.

8.1.26 Tone Status - $CC read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Detected Selcall tone frequency					x	CTCSS phase		Detected DCS or CTCSS code							

This word holds the current status of the CMX7041 sub-audio and In-band tone sections. This word should be read by the host after an interrupt caused by a DCS, CTCSS or In-band tone event. In Tx mode this register will be cleared to '0'.

b15-11 Detected In-band frequency; identifies the frequency by its position in Table 6 In-band Tones. A change in the state of bits 15 to 11 will cause bit 13 of the Status register ($C6), 'In-band State Change', to be set to '1'.

b10 reserved

b9-8 CTCSS phase change detected 00 0 degrees (normal)
01 120 degrees
10 180 degrees
11 240 degrees
A detected change of phase will cause the CTCSS Interrupt to be asserted in $C6

b7–0 Detected DCS or CTCSS code, identifies the detected sub-audio tone by its position in Table 3 CTCSS Tones or Table 5 DCS 23 Bit Codes.

8.1.27 Audio Tone - $CD: 16-bit write-only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	Audio Tone											

When the required bits of the Mode Control register ($C1) are set an audio tone will be generated with the frequency set by bits (11-0) of this register in accordance with the formula below. If bits 11-0 are programmed with '0' no tone (i.e. Vbias) will be generated when the Audio Tone is enabled.

Frequency = Audio Tone (i.e. 1Hz per LSB)

The Audio Tone frequency must only be set to generate frequencies from 300Hz to 3000Hz.

The host must suppress other Audio band signalling and set the correct audio routing before generating an audio tone and re-enable signalling and audio routing on completion of the audio tone. The timing of intervals between these actions is also controlled by the host µC.

This register may be written to whilst the audio tone is being generated, any change in frequency will take place after the end of the C-BUS write to this register. This allows complex sequences (e.g. ring or alert tunes) to be generated for the local speaker (Tx or Rx via the AUDIO pin) or transmitted signal (Tx via the MOD1/2 pins).

8.1.28 Interrupt Mask - $CE write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	NWR	Rx in	xtcss	ctcss	dcs	Aux ADC2	Aux ADC1	FFSK	Data RDY	Data CRC	2k4	1k2	res	0	PRG

Bit	Value	Function
15	1	Enable selected interrupts
	0	Disable all interrupts (IRQN pin not activated)
14	1	Enable interrupt when a change to the status of the WAT tone or SAME data is detected
	0	Disabled
13	1	Enable interrupt when a change to a In-band tone is detected
	0	Disabled
12	1	Enable interrupt when a valid XTCSS 4-tone set is detected or has finished being transmitted
	0	Disabled
11	1	Enable interrupt when a change to a programmed CTCSS tone is detected
	0	Disabled
10	1	Enable interrupt on a change in the detect status of the DCS decoder
	0	Disabled
9, 8	1	Enable interrupt when the corresponding Aux ADC status bit changes
	0	Disabled
7	1	Enable interrupt when FFSK/MSK data transmission has ended
	0	Disabled
6	1	Enable interrupt when an FFSK/MSK data transfer is required
	0	Disabled
5	1	Enable interrupt when a correct CRC portion of a sized Data Block is received
	0	Disabled
4	1	Enable interrupt when valid 2400baud data is detected
	0	Disabled
3	1	Enable interrupt when valid 1200baud data is detected
	0	Disabled
2	1	*reserved*
	0	Disabled
1	0	Reserved for future use. Leave this bit at '0'.
0	1	Enable interrupt when Prog Flag bit of the Status register changes from '0' to '1' (see Programming register $C8)
	0	Disabled

8.1.29 Reserved - $CF write

This C-BUS address is allocated for production testing and must not be accessed in normal operation.

8.2 Programming Register Operation

In order to support radio systems that may not comply with the default settings of the CMX7041, a set of program register blocks is available to customise the features of the device. It is envisaged that these blocks will only be written to following a power-on of the device and hence can only be accessed while the device is in IDLE mode. Access to these blocks is via the Programming register ($C8).

All other interrupt sources should be disabled while loading the program register blocks.

The Programming register should only be written to when the Programming Flag bit (bit 0) of the Status register is set to 1 and the Rx and Tx modes are disabled (bits 0 and 1 of the Mode Control register both '0'). The Programming Flag is cleared when the Programming register is written to by the host. When the corresponding programming action has been completed (normally within 250µs) the CMX7041 will set the flag back to 1 to indicate that it is now safe to write the next programming value. The Programming register must not be written to while the Programming Flag bit is 0. Programming is performed by writing a sequence of 16-bit words to the Programming register in the order shown in the following tables. Writing data to the Programming register MUST be performed in the order shown for each of the blocks, however the order in which the blocks are written is not critical. If later words in a block do not require updating the user may stop programming that block when the last change has been performed. e.g. If only 'Fine output gain 1' needs to be changed the host will need to write to P4.0, P4.1 and P4.2 only.

The user must not exceed the defined word counts for each block. P4.8 is allocated for production testing and must not be accessed in normal operation.

The high order bits of each word define which block the word belongs to, and if it is the first word of that block:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11 – Bit 0
1	X	X	X	1st data for each block
0	X	X	X	2nd and following data
X	1	0	0	Write to block 0 (12 bit words)
X	1	0	1	Write to block 1 (12 bit words)
X	1	1	0	Write to block 2 (12 bit words)
X	1	1	1	Write to block 3 (12 bit words)
X	0	Write to block 4 (14 bit words)		

8.2.1 Program Block 0 – Modem Configuration:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.0	0	1	0	0	0				FFSK/MSK Frame SynC LSB							
P0.1	0	1	0	0	0				FFSK/MSK Frame SynC MSB							
P0.2	0	1	0	0	0				FFSK/MSK Frame SynD LSB							
P0.3	0	1	0	0	0				FFSK/MSK Frame SynD MSB							
P0.4	0	1	0	0	0				Scramble Seed 1 LSB							
P0.5	0	1	0	0	0				Scramble Seed 1 MSB							
P0.6	0	1	0	0	0				Scramble Seed 2 LSB							
P0.7	0	1	0	0	0				Scramble Seed 2 MSB							
P0.8	0	1	0	0	0				FFSK/MSK Bit Sync LSB							
P0.9	0	1	0	0	0				FFSK/MSK Bit Sync MSB							

Default values:

P0.0	$23	P0.5	$00
P0.1	$CB	P0.6	$00
P0.2	$33	P0.7	$00
P0.3	$B4	P0.8	$55
P0.4	$00	P0.9	$55

This initiates the device with the MSK frame sync pattern of $CB23 and bit sync of alternate '1's and '0's.

$C8 (P0.0-3) MSK Frame Sync

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.0	1	1	0	0	0				FFSK/MSK Frame SynC LSB							
P0.1	0	1	0	0	0				FFSK/MSK Frame SynC MSB							
P0.2	0	1	0	0	0				FFSK/MSK Frame SynD MSB							
P0.3	0	1	0	0	0				FFSK/MSK Frame SynD MSB							

Bits 7 to 0 set the Frame Sync pattern used in Tx and Rx MSK data. Bit 7 of the MSB is compared to the earliest received data. Note that SynT is the inverse pattern of SynC.

$C8 (P0.4-7) Scramble Seed 1 and 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.4	0	1	0	0	0				Scramble Seed 1 LSB							
P0.5	0	1	0	0	0				Scramble Seed 1 MSB							
P0.6	0	1	0	0	0				Scramble Seed 2 LSB							
P0.7	0	1	0	0	0				Scramble Seed 2 MSB							

These bits set the scramble seed used on all data bits following a Frame Head. If $0000 is programmed as the seed then no scrambling will occur when selected. If either programmable scramble seeds are selected, both the transmit and receive devices must use the same seed pattern for data to be transferred correctly.

$C8 (P0.8-9) MSK Bit Sync

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.8	0	1	0	0	0				FFSK/MSK Bit Sync LSB							
P0.9	0	1	0	0	0				FFSK/MSK Bit Sync MSB							

This bit pattern is used when transmitting the bit sync portion of a Frame Head.

8.2.2 Program Block 1 – XTCSS and In-band Tone Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Audio band tones / data Tx level											Emph
P1.1	0	1	0	1	XTCSS tone length	Audio band detect threshold							In-band tone detect bandwidth			
P1.2	0	1	0	1	User Programmable Selcall Tone 0											0
P1.3	0	1	0	1	User Programmable Selcall Tone 1											0
P1.4	0	1	0	1	User Programmable Selcall Tone 2											0
P1.5	0	1	0	1	User Programmable Selcall Tone 3											0
P1.6	0	1	0	1	User Programmable Selcall Tone 4											0
P1.7	0	1	0	1	User Programmable Selcall Tone 5											0
P1.8	0	1	0	1	User Programmable Selcall Tone 6											0
P1.9	0	1	0	1	User Programmable Selcall Tone 7											0
P1.10	0	1	0	1	User Programmable Selcall Tone 8											0
P1.11	0	1	0	1	User Programmable Selcall Tone 9											0
P1.12	0	1	0	1	User Programmable Selcall Tone A											0
P1.13	0	1	0	1	User Programmable Selcall Tone B											0
P1.14	0	1	0	1	User Programmable Selcall Tone C											0
P1.15	0	1	0	1	User Programmable Selcall Tone D											0
P1.16	0	1	0	1	User Programmable Selcall Tone E											0
P1.17	0	1	0	1	User Programmable Selcall Tone F											0
P1.18	0	1	0	1	Custom Tone 1											0
P1.19	0	1	0	1	Custom Tone 2											0
P1.20	0	1	0	1	Custom Tone 3											0
P1.21	0	1	0	1	Custom Tone 4											0

Default values:

P1.0:	$800	P1.9	$826
P1.1:	$009	P1.10	$8A8
P1.2	$000	P1.11	$944
P1.3	$A84	P1.12	$9E2
P1.4	$5EA	P1.13	$5A0
P1.5	$660	P1.14	$4E8
P1.6	$6C4	P1.15	$BE4
P1.7	$728	P1.16	$544
P1.8	$7A6	P1.17	$B40

$C8 (P1.0) Audio Band Tones Tx Level

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Audio band tones / data Tx level											Emph

Bits 11 (MSB) to 1 (LSB) set the transmitted In-band tone, Audio Tone and FFSK/MSK signal level (pk-pk) with a resolution of AV_{DD}/2048 per LSB (1.611mV per LSB at AV_{DD}=3.3V). Valid range for this value is 0 to 1536.

Bit 0 controls Rx In-band tone de-emphasis. When In-Band tones are enabled in the Mode Control register ($C1), de/pre-emphasis is enabled in the Audio Control register ($C2) and this bit (b0) is set to '1', signals going to the In-band tone detector are de-emphasised in accordance with Figure 8 of the datasheet.

$C8 (P1.1) In-band tone Detect Bandwidth and Audio Band Detect Threshold

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.1	0	1	0	1	XTCSS tone length		Audio band detect threshold						In-band tone detect bandwidth			

XTCSS tone length (bits 11, 10): '00' = 40ms, '01' = 60ms, '10' = 80ms and '11' = 100ms.

- In transmit mode, these set the transmit tone length for each of the 4 tones in an XTCSS sequence.
- In receive mode these bits define the minimum silent prefix and suffix qualification periods for successful reception and they also define the nominal tone decode length. The tone will be decoded if the tone length is up to 1.5 times the programmed tone length, but will not decode if the tone length is greater than twice the programmed length.

The 'detect threshold' bits (bits 9 to 4) set the minimum In-band tone and/or FFSK/MSK signal level that will be detected. The levels are set according to the formula:

$$\text{Minimum Level} = \text{Detect Threshold} \times 3.993\text{mV rms at } AV_{DD} = 3.3\text{V}$$

The In-band tone detected bandwidth is set in accordance with the following table:

					BANDWIDTH	
	Bit 3	Bit 2	Bit 1	Bit 0	Will Decode	Will Not Decode
	1	0	0	0	±1.1%	±2.4%
Recommended for EEA ⇒	**1**	**0**	**0**	**1**	**±1.3%**	**±2.7%**
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%

$C8 (P1.2 – P1.17) User-Programmable Selcall Tones

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.2-17	0	1	0	1	Programmable Selcall Tone											0
					N (see below)							R (see below)				0

These words set the programmable Selcall tones used in transmit and receive. The frequency is set in bits 11-1 for each word according to the formula:

N = Integer part of (0.042666 x frequency)

R = (0.042666 x frequency - N) x 6000 / frequency (round to nearest integer)

Example: For 1010Hz, N = 43, R = 1. The programmed tones must only be set to frequencies from 400Hz to 3000Hz.

$C8 (P1.18 – P1.21) Custom Tones

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.18 - 21	0	1	0	1	Custom Tone											0
					N (see below)							R (see below)				0

These words set the Custom In-band tones used in transmit and receive. The frequency is set in bits 11-1 for each word using the same formula as the programmable Selcall tones (see above).

8.2.3 Program Block 2 – CTCSS and DCS Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	CTCSS and DCS Tx level											
P2.1	0	1	1	0	DCS 24	0	CTCSS and DCS detect threshold						CTCSS detect bandwidth			
P2.2	0	1	1	0	User Defined DCS Code bits 11 – 0											
P2.3	0	1	1	0	User Defined DCS Code bits 23/22 – 12											
P2.4	0	1	1	0	User Defined CTCSS code N						User Defined CTCSS Code R					
P2.5	0	1	1	0	Sub-audio drop out time				0							

Default values:

P2.0	$800	P2.3	$000
P2.1	$008	P2.4	$000
P2.2	$000	P2.5	$000

$C8 (P2.0) CTCSS and DCS TX LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	CTCSS and DCS Level											

Bits 11 (MSB) to 0 (LSB) set the transmitted CTCSS or DCS sub-audio signal level (pk-pk) with a resolution of AV_{DD}/16384 per LSB (0.201mV per LSB at AV_{DD}=3.3V, giving a range 0 to 824.8mV pk-pk).

$C8 (P2.1) CTCSS TONE BW AND LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.1	0	1	1	0	DCS 24	0	CTCSS and DCS detect threshold						CTCSS detect bandwidth			

Bit 11, DCS 24: When this bit is set to '1' 24 bit DCS codes are transmitted and decoded. When this bit is cleared to '0' 23 bit codes are used.

The 'detect threshold' bits (bits 9 to 4) set the minimum CTCSS or DCS signal level that will be detected. The levels are set according to the formula:

$$\text{Minimum Level} = \text{Detect Threshold} \times 2.2\text{mV rms at } AV_{DD} = 3.3\text{V}$$

The CTCSS detected tone bandwidth is set in accordance with the following table:

	Bit 3	Bit 2	Bit 1	Bit 0	BANDWIDTH Will Decode	BANDWIDTH Will Not Decode
Recommended for use with split tones and Tone Clone™	0	1	1	0	±0.5%	±1.8%
	0	1	1	1	±0.8%	±2.1%
Recommended for CTCSS ⇒	**1**	**0**	**0**	**0**	**±1.1%**	**±2.4%**
	1	0	0	1	±1.3%	±2.7%
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%

$C8 (P2.2-3) DCS CODE (LOWER) and DCS CODE (UPPER)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.2	0	1	1	0	DCS Data (bits 11-0)											
P2.3	0	1	1	0	DCS Data (bits 23/22-12)											

These words set the User Defined DCS code to be transmitted or searched for. The least significant bit (bit 0) of the DCS code is transmitted or compared first and the most significant bit is transmitted or compared last. Note that DCS Data bit 23 is only used when bit 11 (DCS 24) of P2.1 is set to '1'.

$C8 (P2.4) User Defined CTCSS Tone

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.4	0	1	1	0	User Defined CTCSS code N						User Defined CTCSS Code R					

Calculate the values of N and R for the desired CTCSS frequency by:

N= integer (0.24 * User Frequency)

R = ((0.24 * User Frequency) –N * 3000 / User Frequency

Eg: for 150.1Hz, N=36, R=1 so P2.6 = $6901

$C8 (P2.5) Sub-audio Drop Out Time

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.5	0	1	1	0	Sub-audio Drop Out Time				0							

The Sub-audio Drop Out Time defines the time that the sub-audio signal detection can drop out before loss of sub-audio is asserted. The period is set according to the formula:

Time = Subaudio Drop Out Time × 8.0ms [range 0 to 120ms]

The setting of this register defines the maximum drop out time that the device can tolerate. The setting of this register also determines the de-response time, which is typically 90ms longer than the programmed drop out time.

$C8 (P2.6) Reserved – do not access

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.6	0	1	1	0	Reserved – set to $6000											

8.2.4 Program Block 3 – AuxDAC, RAMDAC and Clock control:

This block is divided into two sub-blocks to facilitate loading the RAMDAC buffer. Set bit 15 to restart a loading sequence. If bit 10 is set then loading the first ten locations will be skipped. If bit 10 is clear, the first ten locations must be loaded before continuing to the RAMDAC load.

The Internal clk dividers only require modification if a non-standard XTAL frequency is used (see Table 1).

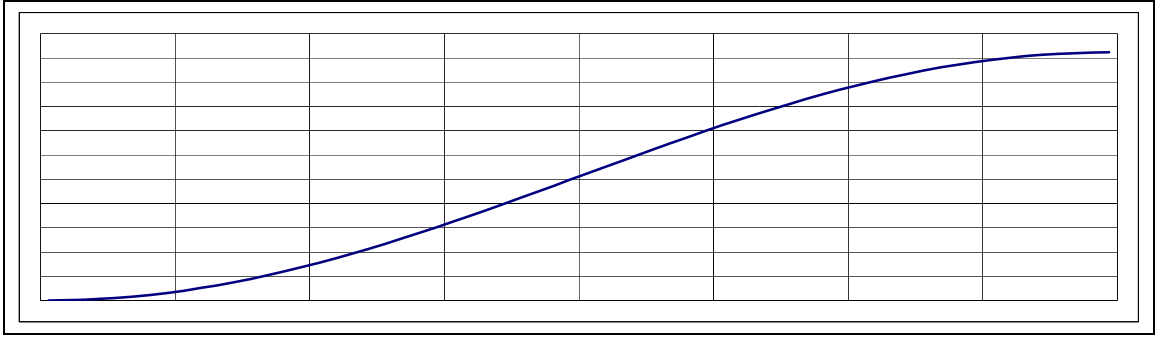
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P3.0	1	1	1	1	0	0	AuxADC1 Average Counter									
P3.1	0	1	1	1	0	0	AuxADC2 Average Counter									
P3.2	0	1	1	1	0	0	GP Timer value in IDLE mode									
P3.3	0	1	1	1	0	0	VCO output and AUX clk divide in IDLE mode									
P3.4	0	1	1	1	0	0	Ref clk divide in Rx or Tx mode									
P3.5	0	1	1	1	0	0	PLL clk divide in Rx or Tx mode									
P3.6	0	1	1	1	0	0	VCO output and AUX clk divide in Rx or Tx mode									
P3.7	0	1	1	1	0	0	Internal ADC / DAC clk divide in Rx or Tx mode									
P3.8	0	1	1	1	0	0	AuxADC Internal Control 1									
P3.9	0	1	1	1	0	0	AuxADC Internal Control 2									
P3.10	0	1	1	1	0	0	AuxADC Internal Control 3									
P3.11	1	1	1	1	0	1	User Defined RAMDAC data 0									
P3.12	0	1	1	1	0	1	User Defined RAMDAC data xx									
P3.75	0	1	1	1	0	1	User Defined RAMDAC data 63									

Default Values:

P3.0	$000
P3.1	$000
P3.2 - P3.7:	see Table 1
P3.8	$000
P3.9	$101
P3.10	$002
P3.11 - P3.75:	see Table 14

Table 14 RAMDAC Values

Default DAC RAM contents after reset (hexadecimal)															
0 000	1 001	2 003	3 006	4 00A	5 010	6 017	7 01F	8 028	9 033	10 03E	11 04B	12 059	13 068	14 078	15 089
16 09A	17 0AD	18 0C1	19 0D5	20 0EA	21 100	22 116	23 12D	24 145	25 15D	26 175	27 18E	28 1A7	29 1C0	30 1D9	31 1F3
32 20C	33 226	34 23F	35 258	36 271	37 28A	38 2A2	39 2BA	40 2D2	41 2E9	42 2FF	43 315	44 32A	45 33E	46 352	47 365
48 376	49 387	50 397	51 3A6	52 3B4	53 3C1	54 3CC	55 3D7	56 3E0	57 3E8	58 3EF	59 3F5	60 3F9	61 3FC	62 3FE	63 3FF



8.2.5 Program Block 4 – Gain and Offset Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain													
P4.1	0	0	Reserved - clear to '0'													
P4.2	0	0	Fine Output Gain 1													
P4.3	0	0	Fine Output Gain 2													
P4.4	0	0	Output 1 Offset Control													
P4.5	0	0	Output 2 Offset Control													
P4.6	0	0	Ramp Rate Control													
P4.7	0	0	Limiter Setting (all '1' s = Vbias +/- AV_{DD} / 2)													
P4.8	0	0	Special Programming Register (Production Test Only)													

Default values:

P4.0	$0000	P4.4	$0000
P4.1	$0000	P4.5	$0000
P4.2	$0000	P4.6	$0000
P4.3	$0000	P4.7	$3FFF

$C8 (P4.0) Fine Input Gain

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain (unsigned integer)													

Gain = 20 × log([32768-IG]/32768)dB. IG is the unsigned integer value in the 'Fine Input Gain' field.

Fine input gain adjustment should be kept within the range 0 to -3.5dB.

$C8 (P4.1) Reserved

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.1	0	0	Reserved - clear to '0'													

This register is reserved and should be cleared to '0'.

$C8 (P4.2-3) Fine Output Gain 1 and Fine Output Gain 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.2	0	0	Fine Output Gain 1 (unsigned integer)													
P4.3	0	0	Fine Output Gain 2 (unsigned integer)													

Gain = 20 × log([32768-OG]/32768)dB. OG is the unsigned integer value in the 'Fine Output Gain' field.

Fine output gain adjustment should be kept within the range 0dB to -3.5dB.

$C8 (P4.4-5) Output 1 Offset and Output 2 Offset

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.4	0	0	2's complement offset for MOD 1, resolution = AV_{DD}/16384 per LSB													
P4.5	0	0	2's complement offset for MOD 2, resolution = AV_{DD}/16384 per LSB													

Can be used to compensate for inherent offsets in the output path via MOD 1 (Output 1 Offset) and MOD 2 (Output 2 Offset). It is recommended that the offset correction is kept within the range +/-50mV.

$C8 (P4.6) Ramp Rate Control

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.6	0	0	Ramp Rate Up Control (RRU)							Ramp Rate Down control (RRD)						

The ramp-up and ramp-down rates can be independently programmed. The ramp rates apply to all the analogue output ports. They only affect those ports being turned on (ramp-up) or turned off (ramp down). The ramp rates should be programmed before ramping any outputs.

Time to ramp-up to full gain = (1 + RRU) × 1.333ms
Time to ramp down to zero gain = (1 + RRD) × 1.333ms

$C8 (P4.7) Transmit Limiter Control

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.7	0	0	Limiter Setting, resolution = AV_{DD}/32768 per LSB													

This unsigned number sets the clipping point (maximum deviation from the centre value) for the MOD 1 and MOD 2 pins. The maximum setting ($3FFF) is +/- AV_{DD}/2 i.e. output limited from 0 to AV_{DD}.

The limiter is only applied to audio signals, not internally generated audio band signals. The levels of internally generated signals must be limited by setting appropriate transmit levels.

$C8 (P4.8) Special Programming Register – do not access.

8.2.6 Initialisation of the Programming Register Blocks:

Removal of the Signal Processing block from reset (b5 1→ 0), with b4 kept low (= 0), will cause all of the Programming register words (P0 – P4) to be reset to their default values.

8.3 Function Image™ Updates

TBD

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